Titre: Title:	Conception pour la testabilité des systèmes biomédicaux implantables
Auteur: Author:	Karim Arabi
Date:	1997
Type:	Mémoire ou thèse / Dissertation or Thesis
Référence: Citation:	Arabi, K. (1997). Conception pour la testabilité des systèmes biomédicaux implantables [Thèse de doctorat, École Polytechnique de Montréal]. PolyPublie. https://publications.polymtl.ca/6780/

UNIVERSITÉ DE MONTRÉAL

CONCEPTION POUR LA TESTABILITÉ DES SYSTÈMES BIOMÉDICAUX IMPLANTABLES

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THÈSE PRÉSENTÉE EN VUE DE L'OBTENTION
DU DIPLÔME PHILOSOPHIAE DOCTOR (Ph.D.)
(GÉNIE ÉLECTRIQUE)

Mai 1997

UNIVERSITÉ DE MONTRÉAL

ÉCOLE POLYTECHNIQUE DE MONTRÉAL

Cette thèse intitulée:

CONCEPTION POUR LA TESTABILITÉ DES SYSTÈMES BIOMÉDICAUX IMPLANTABLES

présentée par: ARABI Karim

en vue de l'obtention du diplôme de: Philosophiae Doctor

a été dûment accepté par le jury d'examen constitué de:

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DÉDICACE

À mes très chers parents

À mon fils, Parsa

À mon épouse

REMERCIEMENTS

Je désire en premier lieu témoigner ma reconnaissance à ma directrice de recherche, Madame Bozena Kaminska, professeure à l'École Polytechnique de Montréal, de m'avoir dirigé et soutenu tout au long de cette thèse, de ses conseils judicieux ainsi que de la disponibilité dont elle a fait preuve.

Je tiens à remercier Messieurs Yvon Savaria et Jean-Jules Brault professeurs à l'École Polytechnique de Montréal et Monsieur Asim Al-Khalili professeur à l'Univesité Concordia d'avoir accepté de participer dans le jury d'examen de cette thèse. Je remercie également Monsieur Georges-Emile April professeur à l'École Polytechnique de Montréal d'avoir participé dans le jury de l'examen général de mon doctorat.

Mes remerciements vont à tous ceux et celles qui, de près ou de loin, ont contribué dans la réalisation de cette thèse. Je remercie aussi tous les personnels du département de génie électrique et de génie informatique de l'École Polytechnique de Montréal.

J'aimerais tout spécialement remercier mes parents pour leurs sacrifices et leur constant encouragement et appui tout au long de mes études. J'adresse également mes remerciements les plus sincères à mon épouse, Shadi.

RÉSUMÉ

Suite au développement initial du stimulateur cardiaque (pacemaker), il y a 35 ans, plusieurs systèmes implantables ont été mis au point pour traiter différentes anomalies. De nos jours, une grande variété de systèmes implantables commercialisés aident à améliorer l'état de santé de nombreux patients, ainsi qu'à sauver des vies. Il s'agit des stimulateurs cardiaques, prothèses cochléaires, prothèses respiratoires, stimulateurs de muscles paralysés, stimulateurs pour contrôler la douleur, systèmes implantables pour l'injection de médicaments, etc.

Les systèmes biomédicaux implantables sont conçus pour satisfaire un ensemble de critères et de performances spécifiques. Il s'agit de la longévité, la biocompatibilité, la reprogrammabilité et flexibilité, une faible consommation, une taille minimale et la fiabilité.

Le progrès technologique considérable des circuits intégrés, et l'avancement indéniable des techniques de traitement clinique utilisant la stimulation électrique ont accéléré l'avènement d'une nouvelle génération de systèmes implantables. Ces systèmes sont multiprogrammables, emploient des boucles de rétroaction et possèdent plusieurs types de capteurs pour capter des informations biologiques et cliniques. Ils sont réalisés en utilisant des circuits électroniques à très grande échelle (VLSI: Very Large Scale Integration) et contiennent des circuits analogiques de haute performance. Cette complexité rend la vérification complète des systèmes implantables très difficile, si la conception pour la fiabilité n'est pas considérée lors de la phase de design du système. De plus, la probabilité d'avoir une panne après l'implantation augmente avec la complexité du circuit électronique implanté. La plupart des systèmes implantables avancés présentent

des lacunes au niveau de la fiabilité. Ils ne profitent même pas des développements dans le domaine de la fiabilité des systèmes d'usage régulier. Vu que l'environnement des implants est l'être humain, le critère de fiabilité doit être strictement respecté.

L'objectif de cette thèse est d'établir une approche globale permettant de vérifier l'état des systèmes implantables et celui du patient avant et après l'implantation. Les techniques efficaces pour la conception des prothèses implantables télétestables et fiables seront donc développées. La même approche peut aussi assurer la biotélémétrie des paramètres biologiques et cliniques. Les informations récupérées permettront, entre autres, la localisation des pannes des circuits électroniques et des électrodes, l'ajustement des convertisseurs numériques/analogiques, l'estimation de la durée de vie de la batterie implantée, l'adaptation du système à l'état du patient, etc.

La plupart des systèmes implantables existants ne sont pas testables une fois implantés, ce qui diminue leur fiabilité. De plus, les techniques de télémétrie qui servent à vérifier l'état du patient sont complexes et requièrent une grande surface de silicium. Alors, la nécessité de mettre au point une méthode simple et pratique pour vérifier l'état du patient et celui du système implantable est urgente.

Afin d'améliorer la fiabilité des systèmes implantables, nous avons procédé de la manière suivante:

1) Développement de méthodes efficaces et simples pour l'autovérification intégrée (BIST: Built-In Self-Test) des circuits mixtes et spécifiquement des circuits implantables. Vu que l'une des causes principales du mauvais fonctionnement des systèmes implantables provient de leur interface bioélectronique, le test des électrodes et fils d'interconnexion a été aussi considéré.

2) Développement des techniques de prédiction de l'occurrence de pannes en utilisant des capteurs de température intégrés et en mesurant la puissance dissipée dans l'implant.

3) Développement d'un nouveau protocole de communication qui assure la transmission fiable de données entre le médecin et l'implant. Ce protocole possède des moyens pour détecter et corriger les erreurs de communication sur place.

Les résultats obtenus au cours de la recherche effectuée dans le cadre de cette thèse vont permettre aux systèmes biomédicaux implantables d'être plus fiables qu'auparavant et de pouvoir bénéficier substantiellement du progrès dans le domaine de l'intégration des circuits électroniques VLSI.

ABSTRACT

Since the initial development of the implantable cardiac pacemaker over thirty five years ago, the field of biomedical engineering has provided many different implantable devices to the medical profession for the treatment of various anomalies. These advances have been possible largely because of the efforts of inventors and entrepreneurs who established an important new industry for biomedical implantable devices. Today, implantable cardioverter and defibrillators, drug delivery systems, neuromuscular stimulators, bone growth stimulators, and other implantable devices are in clinical use and make possible the treatment of a variety of diseases. They save lives and improve the quality of life of many other patients suffering from various medical conditions.

The remarkable progress in the microelectronic integration technology, together with the considerable advancement and maturity of clinical treatment techniques using electrical stimulation, have accelerated the advent of a new generation of implantable devices. They are multiprogrammable and incorporate adjustment and control feedback loops in conjunction with various types of sensors to capture biological and clinical information. The new generations of implantable electronic circuits are fabricated using VLSI technology and incorporate high performance digital and analog building blocks. Functional verification of mixed-signal VLSI circuits is very complicated, unless design for testability (DFT) is considered early during the design procedure. Higher are the complexity and the integration level of an implantable microelectronic circuit, higher is the probability of a fault in the implant. Therefore, the reliability of the new generation of implantable systems becomes more critical and must receive a special attention.

Otherwise, the lack of reliability may lead the physicians to refuse using sophisticated implantable systems in clinical treatments.

The main objective of this thesis is to provide simple and effective methods to design high reliability biomedical implantable devices. Therefore, different aspects of design for reliability are considered. To achieve secure implantable systems, we have focused our efforts in the following research areas.

1) Development of simple and effective methods for built-in self-test (BIST) of mixed-signal circuits and especially implantable systems. As the fault in the bioelectronic interface of implantable systems is an important reason of the implant upset, some techniques to monitor the state of electrodes, leads, and interelectrode tissue are also introduced.

2) Development of techniques to predict the occurrence of eventual faults in electronic systems. Knowing that excessive chip temperatures cause its deterioration, temperature sensors have been integrated with the microelectronic circuit to monitor its thermal state. An on-line power dissipation measurement technique has been also proposed which allow to predict the implant's battery life-time.

3) Development of a new secure communication protocol dedicated to implantable systems having multiple means of error correction capability. This communication protocol can be used for programming the implant and telemetering its parameters as well as the clinical state of the patient.

The results obtained during the research conducted in this thesis will allow the biomedical implantable device to be more reliable and to profit from the remarkable progress in the integration technology of microelectronic circuits. Further developments are necessary to render the implants more reliable, especially in the field of fault tolerant electronic circuit design.

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INTRODUCTION GÉNÉRALE

1.1 GÉNÉRALITÉS

De nos jours, une grande variété de systèmes implantables commercialisés aident à améliorer l'état de santé de nombreux patients ainsi qu'à sauver plusieurs vies. Les systèmes biomédicaux implantables varient du capteur de glucose à la prothèse visuelle. Dans ce chapitre, nous allons brièvement présenter les systèmes implantables existants en portant une attention particulière au stimulateur cardiaque et aux prothèses neuromusculaires. Ce passage nous permettra de soulever les points faibles des systèmes implantables actuels et par conséquent de définir les objectifs généraux de cette thèse afin de trouver les solutions efficaces pour une partie de ces problèmes.

1.2 ARCHITECTURE GÉNÉRALE DES SYSTÈMES IMPLANTABLES

Avant de détailler les différentes applications des systèmes implantables, nous présentons une architecture globale d'un système implantable qui peut être adapté à la plupart des applications. La figure 1 illustre un diagramme bloc global de systèmes implantables qui a le potentiel d'être dédié à toutes les applications cliniques qui requièrent un implant. Le système est basé sur le couplage inductif pour alimenter et programmer l'implant et un couplage optique infrarouge pour la télémétrie et retour de l'information de l'implant vers

le monde extérieur. Il peut aussi avoir une pile au lithium pour alimenter une partie de l'implant pour certaines applications.

Cet implant est constitué de trois parties essentielles: le contrôleur externe, le couplage inductif et/ou optique et l'implant. La description de chaque partie est donnée dans les paragraphes suivants.

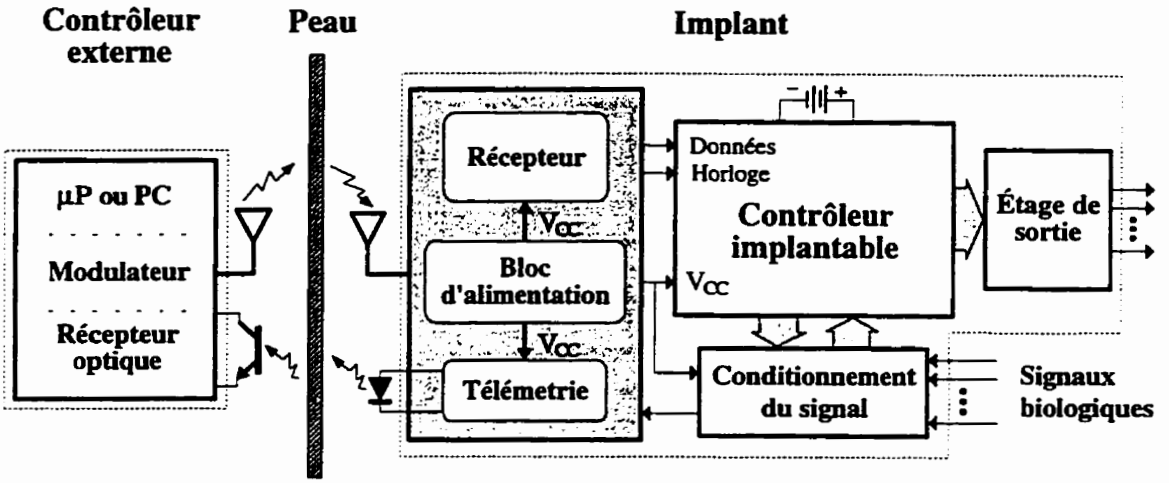

Figure 1: Schéma bloc d'un système implantable pouvant être adapté à différentes applications thérapeutiques.

1.2.1 Contrôleur externe

Le contrôleur externe sert à reprogrammer l'implant pour adapter les différentes fonctions de l'implant à l'état du patient et aux progrès dans les techniques de traitement clinique. Selon le cas, il peut lire l'état du patient, spécifier les paramètres de stimulation, la configuration des électrodes, la quantité du médicament à injecter, les paramètres cliniques à guider etc.. Ce contrôleur englobe:

1) Un processeur qui peut être soit un ordinateur personnel, soit un microcontrôleur qui prépare les paramètres de l'implant en format sériel afin de les envoyer à l'implant via le lien inductif.

2) Un modulateur et transmetteur (lien électromagnétique) qui sert à envoyer l'information et l'énergie vers l'implant. Afin d'assurer la synchronisation, la transmission de l'énergie et de l'information doivent être accompagnées par un signal d'horloge.

3) Un récepteur optique qui recueille les informations envoyées par l'implant. Le couplage optique est réalisé par des ondes infrarouges.

Le contrôleur externe alimente l'implant par le biais de lien inductif pendant la programmation, le fonctionnement de l'implant et la télémétrie. Il faut mentionner que le patient peut aussi posséder un contrôleur simple qui peut transmettre de l'énergie à l'implant via le lien inductif et activer les fonctions de l'implant. Pour des raisons de fiabilité, le contrôleur du patient n'est généralement pas capable de reprogrammer l'implant.

1.2.2 Couplage inductif et optique

Vu qu'il n'existe pas un contact physique entre le contrôleur externe et l'implant, un couplage inductif est utilisé pour établir la communication entre le contrôleur externe et la prothèse implantée. La transmission de l'énergie vers l'implant peut aussi être réalisée par le biais du couplage inductif. Afin de minimiser l'interférence et d'optimiser le rendement, un couplage optique infrarouge est utilisé pour le retour de l'information dans les systèmes avancés.

1.2.3 Implant

L'implant constitue la partie la plus important du système. Il peut être subdivisé en six blocs essentiels:

1) Un récepteur pour récupérer l'onde électromagnétique contenant les données et l'information.
2) Un bloc d'alimentation pour reconstituer une tension d'alimentation stable à partir de l'onde électromagnétique d'entrée;
3) Un contrôleur central qui gère toutes les fonctions de l'implant;
4) Un étage de sortie pour faire l'interface avec le milieu biologique.
5) Des circuits de conditionnement des signaux biologiques;
6) Un bloc de télémétrie pour informer le médecin sur l'état du patient ainsi que celui de l'implant.

La grande majorité des systèmes implantables a été utilisés dans le domaine de la stimulation électrique. Il est donc opportun de donner un survol de cette technique importante qui vient s'imposer dans plusieurs applications thérapeutiques en médecine.

1.3 PRINCIPES DE STIMULATION ÉLECTRIQUE

La stimulation électrique joue un rôle important dans le domaine médical et surtout au niveau de la réhabilitation. Le stimulateur cardiaque est un exemple typique de cette catégorie très importante des circuits biomédicaux implantables basés sur l'électrostimulation. Avant d'introduire les différents types de stimulateurs

neuromusculaires, il est nécessaire de présenter les principes fondamentaux de stimulation électrique.

1.3.1 Principes du système nerveux

Afin de mieux comprendre comment les stimulateurs musculaires et neuromusculaires interagissent dans le corps humain, il sera utile de donner certaines notions de base du contrôle nerveux, en mettant l'accent sur les phénomènes bioélectriques telle la transmission de l'information par le biais des synapses.

1.3.1.1 Les fonctions du système nerveux

Les fonctions principales du système nerveux sont: 1) une fonction sensorielle, 2) une fonction d'intégration 3) une fonction motrice. [64],[97]. Le système nerveux est donc responsable de la perception sensorielle, de l'élaboration de la pensée et de la régulation des fonctions de l'organisme.

Pour accomplir ces activités, le système nerveux recueille d'abord des informations sensorielles provenant de plusieurs terminaisons nerveuses spécialisées dans la peau, les tissus profonds, les yeux, les oreilles et d'autres organes récepteurs. Par l'intermédiaire des nerfs périphériques, ces informations sont acheminées à la moelle épinière et au cerveau qui peuvent immédiatement émettre des ordres moteurs aux muscles. Cette réponse est nommée réponse motrice. L'activation nerveuse des organes internes, à titre d'exemple, l'augmentation du rythme cardiaque ou du péristaltisme intestinal, peut être une composante de cette réponse motrice.

1.3.1.2 Le neurone, le nerf et la transmission synaptique

Le neurone représente la structure unique qui permet la conduction de l'influx nerveux. La figure 2 montre le structure générale des neurones.

Signalons ici que le neurone comprend trois parties, un corps cellulaire ou *soma* et deux types de prolongement: les dendrites qui reçoivent les influx nerveux provenant d'autres neurones et les acheminent vers le corps cellulaire, et l'axone qui transmet l'influx du neurone à d'autres neurones

Des zones fonctionnelles appelées synapses ont la tâche d'établir la communication entre les éléments excitables. Les synapses se trouvent soit entre deux neurones, soit entre un neurone et une cellule effectrice comme au niveau de la jonction neuromusculaire. L'élément nerveux fournissant l'information au niveau de la synapse est appelé présynaptique et l'élément qui reçoit l'information est dit postsynaptique.

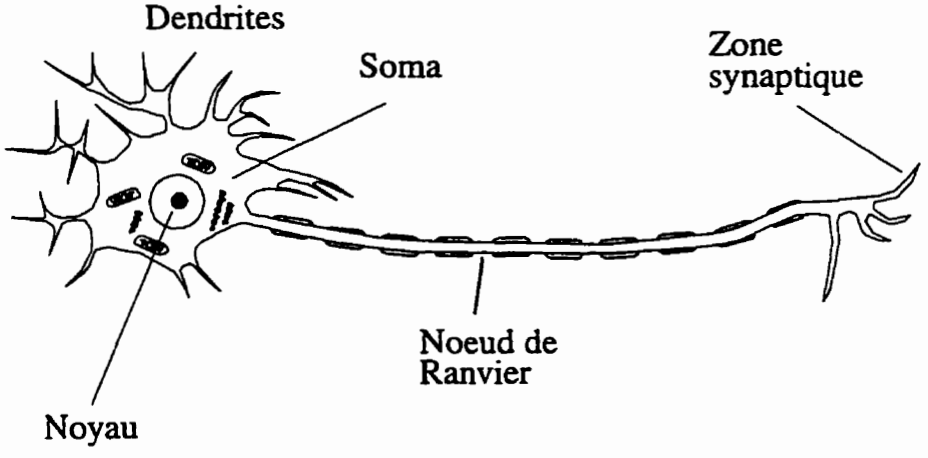

Figure 2: Structure générale des cellules nerveuses.

Au niveau d'une synapse électrique, l'information est transmise directement de l'élément présynaptique à l'élément postsynaptique par l'entremise de courants électriques [64],[97]. En effet, les cellules nerveuses utilisent aussi un autre type de synapse pour communiquer, qui s'appelle synapse chimique. La synapse chimique implique la libération d'une substance neuro-effectrice par l'élément présynaptique. La transmission se fait donc uniquement de l'élément présynaptique à l'élément postsynaptique, tandis que dans une synapse électrique, la transmission se réalise dans les deux directions [64],[97].

Un nerf contient un nombre considérable d'axones et de dendrites regroupées en faisceaux. De plus, chacune des axones et des faisceaux possède sa propre protection.

1.3.2 La stimulation électrique du système neveux

Vu que la stimulation électrique du système nerveux est la méthode habituellement utilisée lors d'expériences de laboratoire et de traitements médicaux pour stimuler les nerfs et les muscles [2],[64] nous étudierons cette méthode dans la section suivante.

1.3.2.1 L'historique de la stimulation électrique

Il y a plus de 2000 ans, des poissons électriques étaient utilisés pour traiter les douleurs ainsi que d'autres maux. C'est en 1791 que Luigi Galvani décrirait l'action de la décharge électrique sur le coeur et les muscles de la grenouille. Un autre chercheur réputé dans le domaine électrique, Alessandro Volta, n'était pas tout à fait d'accord avec la conclusion de Galvani et définit la source de stimulation comme étant une pile créée entre deux métaux différents, d'où vient le principe de première pile électrique [83]. Par la suite, en 1820, Vassall trouvait que la stimulation électrique entraînait un changement du rythme

cardiaque [113]. Ce n'est qu'en 1958 que Senning et Elmaquist construisent le premier stimulateur totalement implantable. En 1965, suite à la théorie de la douleur, Melzack et Wall [86] indiquent que les impulsions douloureuses peuvent être bloquées par une stimulation tactile ou électrique, mettant en jeu les grosses fibres nerveuses myélinisées. En 1967, Shealy [116] rapporte les premiers cas d'implantation d'électrodes le long des cordons postérieurs de la moelle. En 1972, Terry et Davies présentent le premier stimulateur programmable [137]. L'histoire qualifiera probablement les années 1980 comme l'ère des premiers microstimulateurs programmables multimodes. Aujourd'hui, plusieurs sortes de stimulateurs neuromusculaires commercialisés facilitent la vie de nombreux patients et la recherche continue afin d'améliorer la qualité des traitements. Le stimulateur cardiaque est reconnu comme l'une des découvertes technologiques les plus importantes du vingtième siècle.

1.3.2.2 Types des électrodes et courant cathodique et anodique

La tâche d'une électrode dans la stimulation électrique du système nerveux est soit d'injecter la charge électrique ou de la récupérer. L'électrode qui injecte un courant électrique dans la fibre nerveuse est appelée anode et celui qui récupère la charge électrique injectée est dit cathode. Les fibres nerveuses qui sont dans la proximité de la cathode sont stimulées, mais par contre, au niveau de l'anode, les fibres nerveuses deviennent plus réfractaires que normalement à l'excitation. Un courant cathodique est alors en mesure d'exciter une fibre nerveuse tandis qu'un courant anodique l'inhibe.

La figure 3 montre la configuration des électrodes monopolaire, bipolaire et tripolaire. Dans le cas de l'électrode monopolaire, le chemin de retour de courant est établi par une grande électrode placée quelque part dans le corps.

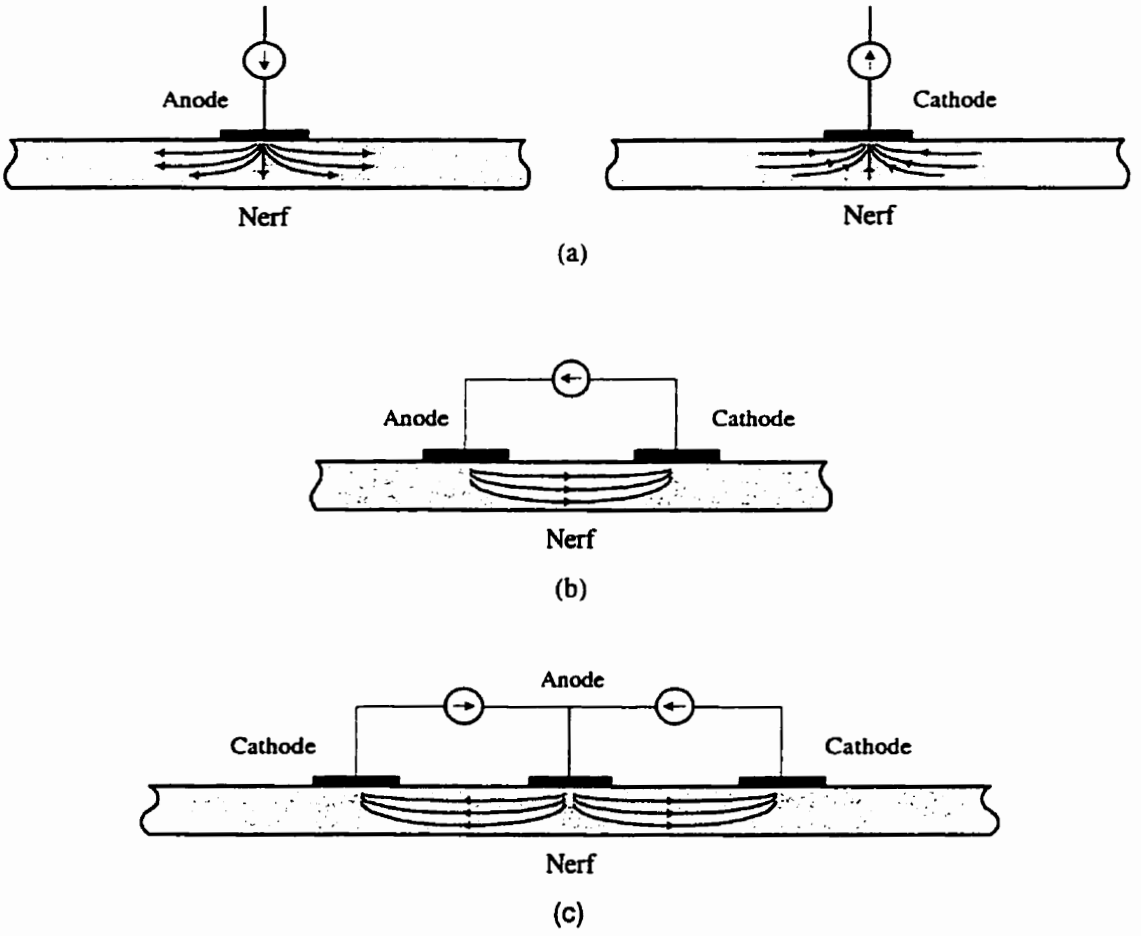

Figure 3: Électrodes de stimulation monopolaire (a), bipolaire (b) et tripolaire (c).

Quel que soit le type de stimulation électrique, le facteur principal est la densité de charge (σ_q) qui est le rapport entre le courant moyen et la surface réelle de stimulation de l'électrode. La densité de charge est exprimée en fonction de la charge par phase (Q_T) et de l'aire géométrique de contact électrode-nerf (S_E) comme suit.

$$\sigma_q = \frac{Q_T}{S_E} = \frac{\int_0^T Idt}{S_E} = \frac{IT}{S_E} \qquad (1)$$

où I représente le courant de stimulation et T est la durée active de la phase stimulante.

1.4 CHAMPS D'APPLICATION DES SYSTÈMES IMPLANTABLES

La diversité des applications des systèmes implantables prend toute son importance dans le domaine médical. Beaucoup de systèmes ont été conçus pour l'usage médical et d'autres sont en phase de développement. Ils peuvent être classifiés sous trois grandes catégories: 1) les microstimulateurs neuromusculaires, 2) les capteurs et appareils de diagnostic 3) les systèmes pour l'injection de médicament.

Cependant, la majorité des implants présentement en utilisation sont dans la première catégorie. Une description brève de chaque type d'implant est donnée dans les sections suivantes.

1.4.1 Les microstimulateurs neuromusculaires

Plusieurs stimulateurs neuromusculaires améliorent la qualité de vie ou peuvent même sauver la vie de patients handicapés lors de traitements cliniques. Ils ont également apporté de nouveaux espoirs et un progrès thérapeutique énorme pour des milliers de patients souffrant de différentes dysfonctions neuromusculaires.

1.4.1.1 Le stimulateur cardiaque (pacemaker)

Ce stimulateur sert à régulariser les activités cardiaques. Les stimulateurs cardiaques sont considérés comme les implants les plus avancés au niveau de la technologie et leurs résultats cliniques s'avèrent très satisfaisants [39],[75],[131],[135]. Outre l'application de nouveaux concepts, le principal moteur de l'évolution des appareils de stimulation

cardiaque a été la recherche d'une fiabilité sans cesse améliorée, alliée à une concurrence certes impitoyable, mais combien stimulante des différentes firmes industrielles.

En 1960, le premier stimulateur cardiaque implantable alimenté par 10 piles au mercure est apparu. C'était un monstre prévu pour une durée de vie de 10 ans. Bien entendu, il ne l'atteignit pas. Il fut victime de presque tous les problèmes qui allaient se poser et qui allaient partiellement être résolus dans les dix ans à venir: problèmes de fiabilité électrique, de fiabilité des piles, de l'encapsulation, du poids et de la taille. Tous ces problèmes sont d'ailleurs interdépendants.

Sur le plan électronique, le stimulateur cardiaque implantable n'aurait pas été possible sans la découverte du transistor. Jusqu'à il y a une quinzaine d'années, les circuits de stimulateurs étaient simples, quelques transistors, condensateurs et résistance réunis par un câblage simple, le tout était noyé dans des résines époxy. La fiabilité de ces premiers appareils était médiocre. Il fallut une dizaine d'années pour comprendre la source de certaines pannes dues aux micro-infiltrations d'humidité ou au dégazage des piles au mercure. C'est en 1972 qu'apparaissent les premiers boîtiers en titane complètement étanches qui allaient se généraliser et s'améliorer au fur et à mesure que la technologie de soudure évoluait. En même temps, les circuits intégrés faisaient leur apparition, plus petits, ils pouvaient dès 1972 être encapsulés dans des petits boîtiers étanches et ils permettaient déjà la diminution de la taille et du poids des boîtiers.

Ces circuits intégrés, d'abord simples (SSI: Small Scale Integration), puis plus compliqués (MSI: Medium Scale Integration), et enfin très complexes (VLSI: Very Large Scale Integration) pour aboutir au microprocesseur amènent les stimulateurs à l'âge adulte en permettant de diminuer la consommation, l'encombrement des circuits, en permettant d'augmenter les fonctions des stimulateurs.

Depuis 1978, la multiprogrammabilité par télémétrie était acquise et utilisée à grande échelle, alors que l'idée était déjà appliquée dès 1970, par Medtronic, avec des plots accessibles en transcutané par des aiguilles triangulaires permettant de régler la tension et la fréquence. En 1997, l'intégration de quelques centaines de milliers de transistors dans un circuit se fait de façon routinière. Avec cette complexité, les stimulateurs cardiaques peuvent être asservis à une fonction physiologique double chambre, avec mémoire tout en devenant petits et légers.

1.4.1.2 La prothèse cochléaire

Ce type de prothèse s'adresse aux personnes soufrant de surdité profonde. Il s'agit de compenser cette dysfonction par la stimulation électrique. Le principe de cette réhabilitation consiste à apporter directement au nerf auditif une stimulation reflétant l'environnement sonore par l'intermédiaire d'une ou de plusieurs électrodes implantées dans la cochlée [67],[93],[98],[147]. Jusqu'à date, ce stimulateur constitue le plus grand triomphe de la technologie des prothèses neuromusculaires. On lui prévoit des améliorations futures substantielles. Dans les systèmes les plus récents, un réseau d'électrodes multicontactes placées dans le scalpa tympan de la cochlée est utilisé.

1.4.1.3 Les stimulateurs de muscles paralysés

Ces prothèses visent la récupération de la locomotion et/ou de l'usage des membres des personnes paralysées [18],[21],[50],[52],[53],[79],[100],[118]. Du côté clinique, des recherches au niveau de la récupération de la locomotion, du contrôle de la posture et de la récupération fonctionnelle ont donné lieu à des résultats impressionnants chez les

blessés médullaires. Les chercheurs utilisent maintenant des appareils complètement implantables, alimentés et contrôlés de l'extérieur du corps.

La stimulation électrique fonctionnelle est une méthode de stimulation organisée en patron, qui est appliquée aux muscles paralysés dans le but d'améliorer la fonction à la suite, par exemple, d'une hémiplégie ou d'une lésion médullaire. La boucle de rétroaction peut être ajoutée aux systèmes de stimulation électrique fonctionnelle pour tenir compte d'informations provenant: 1) de capteurs externes, 2) de l'EMG (électromyographe) de muscles volontaires ou stimulés, 3) de nerfs sensoriels ou 4) des aires motrices du cerveau.

1.4.1.4 La prothèse urinaire

La coordination de deux importants composants nerveux est nécessaire pour assurer la continence aussi bien que la miction. Le premier composant est le système nerveux autonome qui innerve le muscle lisse de la vessie et de l'urètre et le second est le système nerveux somatique qui innerve les muscles du sphincter et du plancher pelvien. Une lésion médullaire peut entraîner divers changements dans certains composants, sinon tous les composants de ce contrôle neural. Le traitement clinique du dysfonctionnement de la vessie et du sphincter vésical se fonde sur diverses stratégies faisant appel à la chirurgie, à la pharmacologie et à la stimulation électrique. Plusieurs types d'implants basés sur les techniques de stimulation électrique introduite dans la section précédente, ont été développés soit:

1) les myostimulateurs où les stimulations électriques sont appliquées directement sur le détrusor et le sphincter [37],[101],

2) les neurostimulateurs qui agissent par l'intermédiaire des nerfs destinés à la commande de la vessie [22],[23],[26],[27],[31],[46],[109].

1.4.1.5 Le traitement de la douleur

La stimulation percutanée afin de contrôler la douleur à l'étage médullaire et supra-médullaire a fait d'énormes progrès. Il a été démontré que les fibres de gros diamètre ont, au niveau de la moelle, une action inhibitrice sur les influx nociceptifs [72],[112],[115]. Le neurostimulateur est donc conçu pour délivrer des stimuli électriques visant à stimuler les fibres nerveuses de gros diamètre, donc à renforcer les mécanismes d'inhibition des influx nociceptifs au niveau de la moelle.

1.4.1.6 La prothèse respiratoire

La neurostimulation du nerf phrénique donne de bons résultats chez les patients souffrant d'insuffisance respiratoire réactivant ainsi la ventilation. Grâce à cette technique, certains malades ont pu reprendre une vie normale [21],[44].

1.4.1.7 La stimulation du cervelet

La stimulation chronique du cervelet des patients atteints d'épilepsie a pour objet d'induire l'activité inhibitrice des cellules de Purkinje. Cette méthode est tentante. Elle s'adresse à des épilepsies de tout genre, particulièrement celle résistante au traitement médical, en utilisant une méthodologie assez univoque et non destructrice [42].

1.4.1.8 La prothèse visuelle

Ce stimulateur utilise la stimulation électrique du cortex occipital en vue d'une réhabilitation de la vision. Les méthodes en cours d'études n'ont pas atteint, au niveau

pratique, une assez grande efficacité pour qu'elles soient utilisées, or, cette application demeure encore au stade de la recherche [32],[35].

D'autres applications peuvent être énumérées pour les microstimulateurs, telles le défibrillateur implantable, le stimulateur destiné à accélérer la guérison des blessures, le stimulateur permettant la croissance des os, etc.

1.4.2 Les capteurs et appareils de diagnostic

À peu près partout dans le corps humain, il existe des milliers de capteurs miniaturisés qui captent de l'information de l'environnement externe et les événements de l'intérieur du corps et les envoient vers le cerveau ou la moelle épinière. Suivant le même principe, plusieurs capteurs intégrés implantables ont été utilisés pour capter de l'information concernant les conditions des différents paramètres biologiques dans le corps pour l'envoyer au médecin par le biais d'un lien de télémétrie ou à l'implant lui-même pour établir une boucle de rétroaction [57],[60],[70],[88],[92],[109],[129],[130]. De nos jours, plusieurs types de stimulateurs cardiaques ajustent le rythme cardiaque en fonction des besoins du corps. L'application des capteurs dans les prothèses à boucle de rétroaction comprend le contrôle de la main et de la locomotion chez des patients handicapés, le coeur artificiel, le contrôle de la tension sanguine, la récupération des fonctions de la vessie et l'injection de médicaments.

Par exemple, dans le cas de la stimulation électrique fonctionnelle, pour la réadaptation à la marche chez les blessés médullaires, différents types de capteurs sont utilisés pour capter 1) les événements externes, 2) électromyographie (EMG) de muscles volontaires ou stimulés, 3) de nerfs sensoriels ou 4) des aires motrices du cerveau. Ces informations prévenant des capteurs peuvent être envoyées au médecin ou être utilisées

dans l'implant pour établir une boucle de rétroaction dans un contrôleur classique (proportionnel, différentiel, intégral, etc.) ou un contrôleur basé sur la logique flou. En général, le contrôleur est basé sur un ensemble de règles fondées sur la connaissance experte, ou diverses méthodes d'apprentissage automatiques telles que les réseaux neuraux, l'apprentissage inductif ou les réseaux sémantiques adaptatifs.

Les implants biotélémétriques sont utilisés pour mesurer des paramètres physiologiques avec le minimum de dérangement pour le patient dans une phase chronique de traitement clinique. Les progrès de la technologie de microfabrication ont donné la possibilité de réaliser des systèmes de mesure stables, miniaturisés et précis, qui sont capables de surveiller l'état du patient.

1.4.3 Les systèmes pour l'injection de médicaments

L'idée principale derrière ce type de système implantable est très simple. Le traitement clinique des maladies qui requièrent l'utilisation chronique et régulière de médicament peut bénéficier de la présence d'un implant qui injecte le médicament directement dans la région d'intérêt au point de vue physiologique. À cause de sa capacité limitée, l'implant est rechargé régulièrement en utilisant une aiguille. Idéalement, l'implant doit être contrôlé par le lien inductif ou optique et alimenté par une source d'énergie de longue-durée. Les applications évidentes de cette technologie comprennent le traitement du diabète, la chimiothérapie pour les patients soufrant de cancer et injection du médicament pour calmer les douleurs chroniques. Les avantages majeurs sont l'administration régulière et précise de médicaments et la diminution des effets secondaires en les administrant juste dans la région d'intérêt.

Depuis 1970, plusieurs systèmes implantables pour l'injection de médicaments ont été développés. Les résultats préliminaires de ces composants sont très encourageants. À titre d'exemple, les patients souffrant de cancer peuvent être traités avec des effets secondaires réduits parce que le médicament peut être appliqué directement à la région contaminée et par conséquent une dose globale plus petite est nécessaire.

1.5 LES PARTICULARITÉS DES CIRCUITS IMPLANTABLES

Les circuits et systèmes électroniques implantables doivent être réalisés avec une attention particulière, car ils sont adressés directement à l'être humain. Ils doivent posséder un ensemble de performances particulières, soit la longévité, la biocompatibilité, la reprogrammabilité et la flexibilité, une faible consommation, une taille minimale et la fiabilité.

Plusieurs de ces critères sont nécessaires afin de s'assurer que le circuit ne posera pas de problème une fois qu'il sera implanté dans le corps.

1.5.1 Longévité

La longévité est grandement affectée en premier lieu par la durabilité de la pile, par le milieu biologique très agressif dans lequel l'implant devra fonctionner, et finalement par les défectuosités de l'implant. Pour certaines applications, l'implantation d'une pile demeure indispensable. Plusieurs équipes de recherche ont contribué à augmenter la longévité des stimulateurs. L'histoire de l'évolution des sources d'énergie interne s'est faite plutôt dans le domaine de la stimulation cardiaque. Parmi ces activités, certaines approches comme l'utilisation de l'activité musculaire et de l'activité biophysique [92] se sont soldées par des

échecs complets. Le premier stimulateur rechargeable réalisé et commercialisé par Pacesetter en 1997 fut un échec à cause de la durée de vie limitée des piles rechargeables. Les piles nucléaires ont l'avantage d'avoir une durée de vie plus longue. Le stimulateur nucléaire de Laurens (1970) construit par Alcatel-Medtronic® réitère une réalisation de prestige, très vite minimisée par le prix, le volume, la fiabilité, les difficultés administratives liées à son utilisation et surtout par l'utilisation d'une pile au lithium. Cependant, la pile au lithium a gagné définitivement la compétition, après que General Electric® a abandonné le projet d'une pile au mercure après l'avoir annoncée et réalisée. La durée de vie de pile au mercure a été optimisée à 8 ans.

Aujourd'hui, les piles au lithium ont l'avantage d'avoir une durée de vie plus longue (10 ans pour les stimulateurs à faible consommation) que les piles au mercure et ont un plus faible volume. Elles sont considérées comme étant le meilleur choix de pile pour les circuits implantés.

1.5.2 Biocompatibilité

Afin de protéger le système implantable et le milieu biologique, tout matériel implantable doit être encapsulé. La biocompatibilité des matériaux utilisés pour l'encapsulation est une des principales contraintes des systèmes implantables. Si le matériau et le tissu qui sont en contact n'engendrent pas de changement de leurs propriétés et si le pH sanguin du milieu demeure intact, alors le matériau peut être considéré comme étant biocompatible. La biocompatibilité dépend du matériau, des tissus, ainsi que de l'interaction électrochimique entre eux. Les matériaux doivent être choisis avec soin, afin d'éviter toute contamination du milieu biologique ainsi qu'une corrosion à long terme des circuits et des réactions toxiques ou inflammatoires.

1.5.3 Reprogrammabilité et flexibilité

La reprogrammabilité et la flexibilité diminuent les risques d'être confronté au cas où l'implant devrait être extrait du corps pour modifier ses paramètres de fonctionnement et pour l'adapter à l'évolution du patient et aux techniques de traitement clinique.

La longévité accrue des implants alimentés par des piles au lithium justifie à son tour les implants reprogrammables. En effet, la probabilité d'une modification des besoins du patient s'accroîtra sans doute dans la mesure où le même système reste implanté. Les stimulateurs cardiaques multiprogrammables ont déjà éprouvé la fiabilité de la programmation non invasive.

L'ajustement que procure les implants multiprogrammables servira à l'amélioration de la qualité de vie des patients. En effet, le système sera facilement reconfigurable dans certaines situations cliniques spécifiques. Il sera aussi adaptable aux nouvelles techniques de traitement et aux nouveaux besoins du patient. La programmabilité augmente aussi la sécurité pour le bien-être du malade.

1.5.4 Faible consommation

Pour des systèmes implantables alimentés par des piles, la faible consommation est toujours une caractéristique recherchée et même parfois critique. Une faible consommation permet aux systèmes implantables d'avoir une longévité plus grande ou d'être miniaturisés en utilisant des piles avec des dimensions réduites. Dans le cas de systèmes implantables à source d'énergie externe où un contrôleur externe transmet de l'énergie à travers la peau par l'intermédiaire d'un lien électromagnétique une consommation faible est désirée. Le lien électromagnétique a un rendement faible et une capacité limitée de transmission d'énergie. De plus, la quantité de l'énergie que l'on peut

passer par la peau est limitée par des facteurs de sécurité. On peut donc conclure que dans les systèmes implantables, la consommation doit être réduite autant que possible.

Au point de vue de la consommation d'énergie, la technologie CMOS est considérée comme la seule technologie présentement disponible pouvant convenir aux circuits implantables complexes. La nécessité d'un faible courant de repos rend la technologie CMOS particulièrement attrayante. La principale raison est qu'un élément logique en CMOS statique n'utilise du courant qu'au moment des transitions. Récemment, les chercheurs en microélectronique ont porté une attention très particulière au développement des techniques permettant de concevoir des circuits et des systèmes à faible consommation. En résumé, la diminution du niveau de tension d'alimentation, la diminution des fréquences d'opération et la réduction du nombre de transitions sont des techniques permettant de réduire la consommation d'un circuit.

1.5.5 Taille minimale

La taille et le poids minimaux sont évidemment souhaitables afin de rendre l'utilisation de l'implant le plus transparent possible et de réduire les complications physiques dues à son existence dans le corps. Évidemment, le patient ne désire pas sentir la présence d'un objet étranger à l'intérieur de son corps et ne souhaite pas de déformation à travers la peau. Finalement, une petite taille rend l'intervention chirurgicale plus simple.

1.5.6 Fiabilité

Puisque les implants fonctionnent à l'intérieur du corps humain, la fiabilité doit être sévèrement observée. Toutes sortes de malfonction peuvent sérieusement affecter la vie

ou le bien-être du patient. Un implant, une fois implanté, est complètement inaccessible pour y apporter des ajustements ou des modifications. De plus, le coût de procéder à des interventions chirurgicales pour détecter la source d'un mauvais fonctionnement de l'implant est assez élevé. Les facteurs suivants rendent la fiabilité des implants plus critique que dans le passé:

1) Les progrès cliniques considérables dans les techniques de traitement demandent aussi des systèmes implantables plus avancés. De nos jours, la plupart des implants utilisent des boucles de rétroaction et possèdent plusieurs types de capteurs pour capter des informations biologiques. Ces options exigent la présence des circuits analogiques de haute performance et de contrôleurs puissants pour traiter et gérer les informations. De plus, les progrès récents des technologies microélectroniques ont permis de réaliser des implants de plus en plus complexes avec un niveau d'intégration plus grand. Ce qui rend leur vérification fonctionnelle beaucoup plus difficile avant l'implantation et impose une probabilité plus grande de rencontrer des pannes électroniques après l'implantation. Dans le but d'augmenter la fiabilité et de minimiser les risques d'erreurs non prévues dans le fonctionnement électronique du circuit, sa testabilité doit être considérée lors de sa conception.

2) Presque tous les systèmes implantables sont reprogrammables. La reprogrammabilité donne un grand degré de flexibilité à l'implant et lui permet de suivre les progrès dans les techniques de traitement clinique et d'être adapté à l'état du patient. La reprogrammation se fait à travers un lien inductif ou optique dans un milieu assez bruité. Si la perturbation affecte la communication, l'implant peut être mal programmé, et par conséquent il ne fonctionnera pas comme on le désire. C'est pourquoi il est très important de prévoir un protocole de

communication assurant une probabilité assez basse d'avoir un message erroné. Afin d'assurer la fiabilité de la communication et de minimiser les risques d'erreurs non prévues, des techniques de détection et de correction d'erreurs doit être implantés dans le protocole de communication.

3) La longévité accrue des nouvelles générations des piles et les progrès dans les domaines de la biocompatiblilité et de l'encapsulation permettent aux implants d'avoir une durée de vie plus grande qu'avant. Il est donc primordial de pouvoir vérifier les performances de l'implant après l'implantation, afin de lui assurer un fonctionnement complet.

1.6 TENDANCE FUTURE

Le résultat de notre recherche bibliographique sur les systèmes biomédicaux implantables démontre que les objectifs de la biocompatibilité, la reprogrammabilité, la flexibilité et la taille minimale ont été déjà atteints grâce aux travaux multidisciplinaires de nombreux chercheurs. Quant à la longévité, les implants alimentés par une pile ont une durée de vie de batterie allant jusqu'à environ dix ans et les systèmes alimentés par le lien inductif peuvent rester plus que vingt ans dans le corps humain.

Par contre, le critère de fiabilité, qui devient de plus en plus critique dans les systèmes biomédicaux implantables, semble être négligé. Malheureusement, la technologie des implants n'a même pas suivi les progrès dans le domaine de la fiabilité développé pour les systèmes d'usage régulier. Le manque de fiabilité des systèmes biomédicaux implantables avancés nous a encouragé à consacrer la présente thèse à développer des approches efficaces et surtout simples afin d'améliorer la fiabilité de ces systèmes. Nous

adressons les besoins des implants en général plutôt que de proposer une solution dédiée à un type spécifique de systèmes implantables.

La fiabilité d'un système biomédical implantable peut être amélioré par les solutions suivantes:

1) Développement des techniques de conception pour la testabilité (DFT: Design for Testability) et l'autovérification intégrée (BIST: Built-In Self-Test) convenant aux systèmes implantables.
2) Développement des techniques de prédiction de l'occurrence éventuelle des pannes, surveillance de batterie et mesure de puissance dissipée. Ces techniques permettront de prévenir des pannes éventuelles et d'estimer précisément la durée de vie des batteries.
3) Établissement d'un chemin de retour de l'information (télémétrie) pour informer le contrôleur externe sur l'état du système implanté ainsi que celui du patient.
4) Développement d'un protocole de communication fiable dédiée aux systèmes biomédicaux implantables, permettant de détecter et de corriger les erreurs de communication introduites par le couplage inductif ou optique.
5) Développement des circuits biomédicaux tolérants aux pannes. Ces circuits utilisent normalement un grand degré de redondance afin de corriger sur place l'effet de la panne introduite.

Les quatre premiers points sont couverts dans les prochains chapitres de cette thèse. La conception des circuits biomédicaux tolérants aux pannes exige d'autres recherches détaillées. En effet, la conception des circuits numériques tolérants aux pannes

est assez mature. Cependant, le problème n'a pas été encore abordé dans les circuits analogiques.

Le reste de cette thèse est complétée comme suit. Dans le chapitre 2, nous allons présenter la solution retenue pour le test de la partie numérique des systèmes implantables. Des solutions efficaces et pratiques seront proposées pour le test de la partie analogique dans le chapitre 3. Le problème de test et la vérification des électrodes et les fils d'interconnexion des implants appelés aussi interface bioélectronique seront abordés dans le chapitre 4. Le chapitre 5 discute de la prédiction des pannes et de la mesure continuelle de la dissipation de puissance. Finalement, un protocole de communication dédié aux systèmes biomédicaux sera introduite dans le chapitre 6. La thèse se termine par une conclusion globale.

1.7 CONCLUSION

Au cours de ce chapitre, un survol des différentes applications et l'état de l'art des systèmes biomédicaux implantables a été présentée. Les particularités et spécifications exigées pour les implants ont donc été discutées et les lacunes des systèmes existants ont été soulevées. Nous avons conclu que le problème de fiabilité doit être adressé plus en détail à cause de la complexité et aussi de la diversité des capacités de nouvelles générations des systèmes biomédicaux implantables. C'est d'ailleurs ce qui sera présenté aux prochains chapitres.

CHAPITRE 2

CONCEPTION POUR LA TESTABILITÉ DE LA PARTIE NUMÉRIQUE DES CIRCUITS IMPLANTABLES

2.1 Résumé

Le principal problème de test dans la phase de production des systèmes numériques est celui de minimiser le temps de test qui est un facteur principal et dominant dans l'équation de coût de test. En effet, à cause de la complexité élevée des systèmes numériques, il est presque impossible de couvrir toute la fonctionnalité du système dans un budget de temps limité. L'histoire n'oubliera pas les problèmes de testabilité dans les réalisations les plus glorieuses de systèmes numériques qui ont contribué à forcer l'industrie à considérer la testabilité comme un besoin réel, sans quoi l'évolution des circuits intégrés à très grande échelle aurait pu être bloquée. Pour remédier au problème de testabilité, la conception pour la testabilité a été proposée afin d'augmenter la contrôlabilité et l'observabilité des systèmes numériques. Ces caractéristiques permettront de minimiser le temps de test parce que les noeuds internes du circuit sous test peuvent être contrôlés et observés plus facilement.

Aujourd'hui, la conception pour la testabilité des circuits numériques est arrivée à un degré de maturité qui a convaincu la majorité de concepteurs des systèmes numériques de l'adopter comme une étape indispensable du design des systèmes commercialisés afin de diminuer le coût de test et par conséquent le coût de production.

Un autre problème, qui est relié à la testabilité, est celui de la fiabilité. La fiabilité est un facteur essentiel pour des applications critiques comme l'aérospatiale et le biomédical. Parmi les différentes méthodes de test, la technique basée sur la mesure de courant de repos I_{DDQ} est reconnue pour donner une meilleure couverture de pannes pour les défauts éventuels du circuit sous test. Par exemple, un court-circuit dans un circuit sous test augmente considérablement le courant de repos, même si dans certain cas la fonctionnalité du circuit est inchangé. Ce défaut peut éventuellement développer une panne dans le circuit. C'est pourquoi la technique de test I_{DDQ} est plutôt classifiée dans la catégorie des techniques de test pour la fiabilité. Le choix de la technique de test I_{DDQ} pour la partie numérique des systèmes implantables semble donc judicieux.

Dans les circuits VLSI, le courant de repos est assez grand pour masquer l'effet des défauts qui changent légèrement le niveau de courant de repos. Afin de pouvoir appliquer le technique de test I_{DDQ} aux circuits VLSI, il faut utiliser des capteurs de courant intégrés. Dans ce cas, chaque capteur détecte le courant de repos d'une partie de circuit. Malheureusement la majorité des capteurs de courant intégrés ne donnent pas la précision voulue ou affectent le niveau d'alimentation du circuit sous test.

Dans ce chapitre, nous proposons un capteur de courant intégré qui assure la précision de mesure et qui n'affecte pas le niveau d'alimentation pour notre application. Le principe de base est d'intégrer le capteur de courant avec le régulateur de tension du circuit sous test. Ce qui permet de ne pas affecter le niveau de tension du circuit une fois qu'il est régularisé.

Le même capteur a été utilisé pour mesurer continuellement la consommation de puissance dans le circuit sous test. La mesure de consommation de puissance peut être considérée comme un test complémentaire à la technique de test I_{DDQ}, car elle vérifie la

fonctionnalité du circuit sous test durant le fonctionnement, tandis que la technique de test I_{DDQ} vérifie le circuit dans l'état de repos seulement.

La mesure de la consommation de puissance peut aussi être utilisée pour estimer la durée de vie des batteries dans des applications utilisant une source d'énergie autonome.

2.2 "Design and Realization of an Accurate Built-In Current Sensor for I_{DDQ} Testing and Power Dissipation Measurement"

Dans la prochaine section, nous allons proposer une solution pratique pour réaliser des capteurs de courant intégrés afin

Design and Realization of an Accurate Built-In Current Sensor for I_{DDQ} Testing and Power Dissipation Measurement

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Abstract

Built-in current sensor (BICS) is known to enhance test accuracy, defect coverage and test rate of quiescent current (I_{DDQ}) testing method in CMOS VLSI circuits. For new deep-submicron technologies, BICSs become indispensable for accurate and practical I_{DDQ} testing. This paper presents a BICS suitable for on-line power dissipation measurement and I_{DDQ} testing. Although the BICS presented in this paper is dedicated to submicron technologies that require reduced supply voltage, it can also be used for applications and technologies requiring normal supply voltage. The proposed BICS has been extended for on-line measurement of the power dissipation using only an additional capacitor. Power dissipation measurement is important for safety-critical applications and battery-powered systems. A simple self-test approach to verify the functionality and accuracy of BICSs has also been introduced. The proposed BICS has been implemented and tested using an N-well CMOS 1.2 μm technology. Presented results demonstrate that a very good measurement accuracy can be achieved.

1 Introduction

Due to the advances in the fabrication process of integrated circuits and the market requirements, the trend of designing complex application specific integrated circuits (ASIC) has increased. Whilst the complexity of integrated circuits has greatly increased, the number of available I/O pins increased only marginally. Therefore, the controllability and observability have been considerably decreased. To overcome this problem, a number of test pins should be added when using classical test methods which rely on logic testing. It has been shown that logic testing is not effective for bridging faults, such as gate oxide shorts, polysilicon or metal bridges between the circuit nodes, soft *pn* junctions and transistor punch-through, which result in indeterminate logic values. Besides, some physical imperfections, such as open- or short-circuit defects, for example missing metal, improper etching, electromigration, pattering errors, and opens in diffusions or polysilicon due to mask fabrication errors, which do not immediately affect the logic function, cannot be detected. The undetected defects degrade circuit performance and may later provoke logic errors and therefore their presence implies a lower performance and reliability.

In recent years, a new method of testing digital integrated circuits based on monitoring the quiescent state of the supply current (I_{DDQ}) has been proposed [1],[3]. In the quiescent state, CMOS circuits draw a very small current, typically nanoamperes, which is raised by several orders of magnitude in the presence of certain defects. I_{DDQ} testing increases test coverage, since it can observe every circuit node without adding any test points. In this test technique, abnormal quiescent currents often indicate an internal defect, design error, or fabrication failure. Research results indicate that the most commonly encountered physical defects in CMOS circuits cause abnormal quiescent power bus current and are hence detectable using I_{DDQ} testing [4]. In fact, the majority of the above-mentioned defects, and especially bridging faults, are easily detectable by I_{DDQ}

test techniques. I_{DDQ} test was found to be very effective to catch devices subject to infant mortality failure and therefore results in a higher reliability [5]. It can be concluded that for safety critical applications and battery powered devices such as pacemakers, inclusion of I_{DDQ} testing is crucial.

The effectiveness of I_{DDQ} testing depends on the accuracy of measurement equipment and the test rate [3]. Off-chip current sensing techniques that are currently employed in fabrication testing have showed a limited accuracy and speed performance. Nano- to micro-ampere current levels will be corrupted by comparatively large currents in the circuit pad drivers. Built-in current sensors (BICS) overcome the mentioned shortcomings by offering better current discrimination and higher testing speeds [2],[4].

The Semiconductor Industry Association (SIA) road map for the next 15 years focuses on submicron technologies with further decreases in transistor's minimum size down to 0.07 μm and higher transistor integration of up to 1 billion per integrated circuit (IC) [6]. On one hand, the SIA objectives encourage the utilization of I_{DDQ} testing, because in submicron technologies due to the shrinking dimensions, the bridging faults, which are believed to be easily detectable by I_{DDQ} testing but resistant to the logic testing, become much more probable. On the other hand, the SIA road map questions the efficiency of I_{DDQ} testing because of high I_{DDQ} levels of around hundreds of microamperes or even milliamperes per IC due to increasing transistor off-state leakage current and the enormous number of transistors per chip. BICSs can alleviate the problem of high I_{DDQ} on submicron ICs by partitioning the IC to subcircuits so that each part would have a dedicated BICS with a fraction of the total IC current. Therefore, I_{DDQ} testing of submicron technologies requires the development of accurate BICSs.

Unfortunately, most of the presented BICSs affect the supply voltage level of the circuit under test and therefore reduce its speed performance. A brief review of typical

BICSs proposed in the literature has been presented in [9]. They are not specifically aimed at submicron technologies and specific applications that require power supply down conversion. Besides, the majority of existing BICSs are based on the insertion of a resistive element in the power supply current path and sensing the voltage drop across the resistor [1],[7]-[12]. The main inconvenience of this technique is the instability of the CUT's supply voltage level especially in the presence of high transient currents during CUT's normal operation. Supply voltage level variations would result in a reduced noise margin and the speed performance degradation. In this paper, we present an accurate BICS based on current mirroring that keeps the supply voltage level constant in both test and functional modes. The proposed BICS is especially suitable for submicron CMOS technologies.

2 I_{DDQ} Test Built-In Current Sensor Design

Submicron technologies should have a voltage power supply lower than today's 5 V standard to protect them against hot carrier degradation. Therefore, submicron ICs require a supply voltage converter to adapt the standard system supply voltage to their nominal supply voltage which may be between 2 V and 3.5 V depending on the technology and the application. As an on-chip voltage down converter is normally required to provide a suitable supply voltage for submicron ICs, we propose to integrate the current sensor with the voltage down converter which results in many advantages such as a reduced area overhead and an unaffected and stable supply voltage. In the following, we first present the detailed design of an on-chip voltage down converter and then introduce the BICS.

2.1 Voltage Down Converter

The voltage down converter block must provide a stable and precision voltage source for the circuit under test (CUT) during both mission and test modes. The voltage down converter should consume a very small amount of current, yet be able to deliver currents of up to a few milliamperes. Fig. 1 shows the schematic of such a circuit. V_{DD} denotes the system standard supply voltage which should be adapted to the submicron IC's nominal supply voltage V'_{DD} through the voltage regulator shown in Fig. 1(c). Fig. 1(a) represents a precision CMOS voltage reference providing V_{REF}. The produced voltage reference is adapted to the nominal supply voltage of the CUT using the circuit shown in Fig. 1.

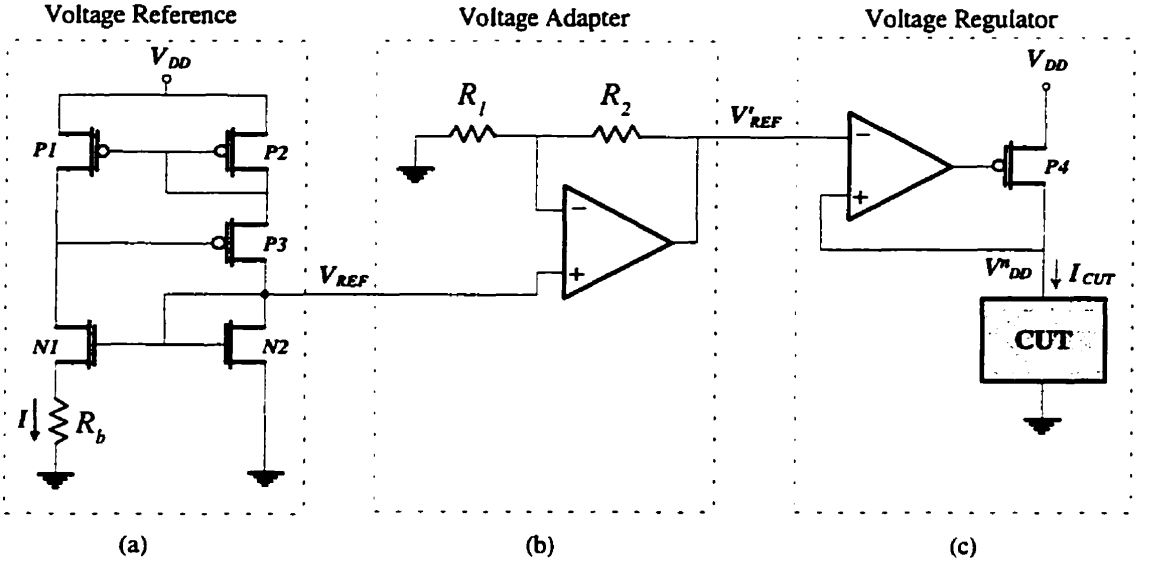


Fig. 1: Circuit schematic of the precision CMOS voltage reference and regulator.

In Fig. 1(a), when every transistor is biased into its active mode, the operating current and reference voltage, ignoring the channel-length modulation effect modeled by λ , are given by [13]:

$$I = \frac{V_{gsN2} - V_{gsN1}}{R_b} = \frac{2\left(\sqrt{\beta_1} - \sqrt{\beta_2}\right)^2}{R_b^2 \beta_1 \beta_2} \tag{1}$$

$$V_{REF} = V_t + \frac{2\left(\sqrt{\beta_1} - \sqrt{\beta_2}\right)}{R_b \sqrt{\beta_1 \beta_2}} \tag{2}$$

where $\beta = \mu C_{OX} \frac{W}{L}$. V_{gs} denotes the gate-source of the MOS transistor, V_t represents the threshold voltage of the transistor, μ is the carrier mobility and C_{OX} is the gate capacity per unit area.

The magnitude of the reference voltage is almost independent of the external supply voltage. The supply voltage dependence can be given as:

$$\frac{\partial V_{REF}}{\partial V_{DD}} = \frac{\lambda_n - \lambda_p}{R_b \sqrt{\beta_1 \beta_2}} \tag{3}$$

where λ_n and λ_p are the channel length modulation parameters of NMOS and PMOS, respectively. We remark that as the channel length gets longer or the resistor R_b becomes bigger, the voltage dependence decreases.

The voltage reference V_{REF} is shifted to V'_{REF} which is equal to the supply voltage of the submicron IC denoted by V''_{DD}. This is performed in the voltage adapter block shown in Fig. 1(b), using a resistive feedback. In Fig. 1(c) the positive and negative inputs of the operational amplifier (opamp) are forced to be equal because of the existence of the negative feedback and very high DC gain of the opamp and therefore

$$V''_{DD} = V'_{REF} = (1 + R_2/R_1)V_{REF} = (1 + K)V_{REF} \tag{4}$$

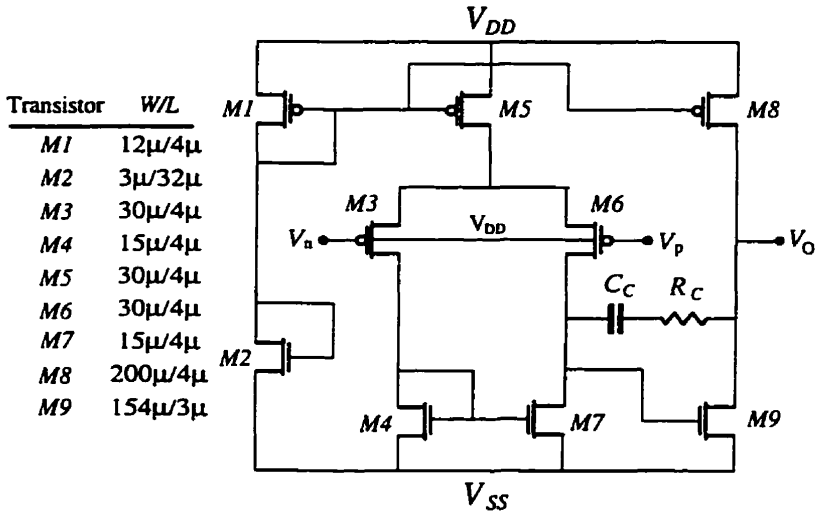


Fig. 2: Compensated CMOS operational amplifier. The opamp unity gain bandwidth (f_T)and its gain at DC (a_V) are 26 MHz and 91.6 dB respectively. R_c = 2 kΩ and C_c = 1 pF.

Low offset voltage, low noise and high input impedance are required for the operational amplifiers. The current consumption of the CUT is provided directly by V_{DD} via transistor *P4*. In order to achieve the best characteristics, and to reduce the equivalent input noise, a PMOS input stage operational amplifier [14] has been employed. PMOS devices present better noise performance than NMOS transistors. The $1/f$ noise contribution by the input transistors has been reduced by increasing their W and L and keeping *W/L* constant. The thermal noise contribution has also been reduced by increasing the transconductance of the input transistors. Fig. 2 shows the schematic representation of the opamp. Experimental results indicate a very good stability and precision of voltage reference (Fig. 3) and the capability of the voltage regulators to drive a wide range of currents (Fig. 4).

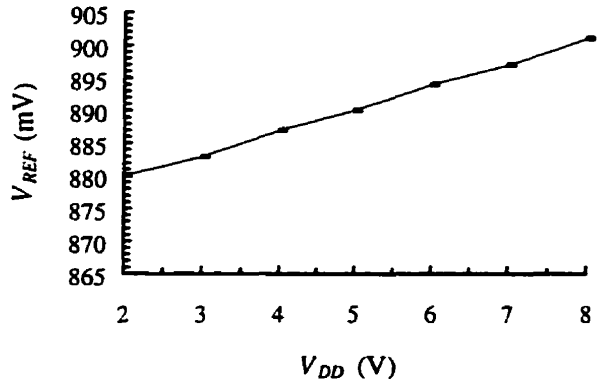


Fig. 3: Voltage dependence characteristics of the reference voltage versus the main supply voltage (V_{REF} = 0.89 V @ V_{DD} = 5 V).

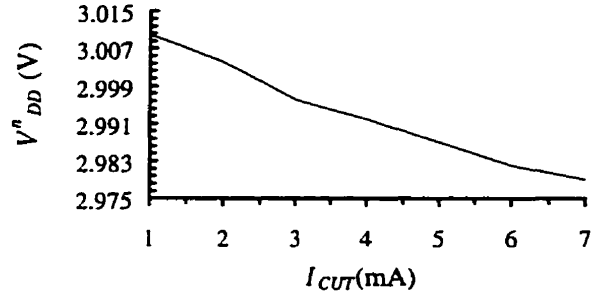


Fig. 4: Output voltage stability of the voltage regulator (V''_{DD}) versus its load current.

2.2 Built-In Current Sensor

Fig. 5 illustrates the proposed current sensor integrated with the voltage down converter. Transistors *P4*, *P5* and *P6* along with the operational amplifier OA2 provide I'_{CUT} which is a scaled copy of the current passing through the CUT (I_{CUT}). The V-I characteristic of transistors *P4* and *P5*, when they are in the linear region ($V_{ds} \leq V_{gs} - V_t$), is given by

$$I_{ds} = \beta\left((V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right) \approx \beta(V_{gs} - V_t)V_{ds} \tag{5}$$

where V_{ds} denotes the drain-source voltage and I_{ds} represents the drain-source current of a transistor. Equation (5) indicates that to establish the same I_{ds} current in both *P4* and *P5* transistors, their V_{gs} and V_{ds} voltages must be equal. Physical connections between their gates and sources makes their V_{gs} voltages identical. The feedback established by OA2 forces the drain voltage of transistors *P4* and *P5*, and consequently their V_{ds} voltages, to be equal resulting in an accurate current sensing even when the transistor *P4* is in the linear region due to the close values of V_{DD} and V'_{DD}.

This is a useful characteristic for the applications where the CUT should be powered by a standard supply voltage. In this case V'_{DD} can be chosen very close to V_{DD}, knowing that the current mirror accuracy is still maintained. As it will be explained later in this paper, the current sensed may be used for either I_{DDQ} testing or on-line power dissipation measurement. In both cases, the measurement element (ME) evaluates the current sensed.

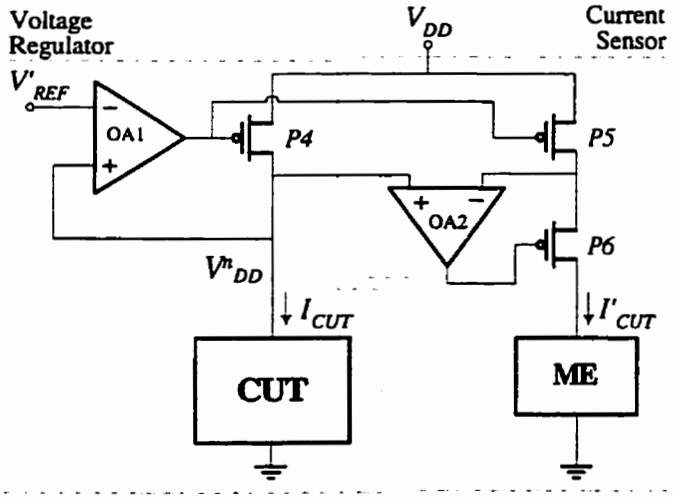


Fig. 5: Block diagram of the current sensor integrated with the implant voltage regulator (ME: Measurement Element).

Fig. 6 illustrates the comparison between the current sensed I'_{CUT} and the CUT's current I_{CUT} for different current levels. The results of simulations demonstrate that the current mirror provides a good accuracy for different current levels. As the equation (4) clarifies, the CUT's nominal voltage V''_{DD} can be adjusted using the ratio $K = R_2/R_1$. Fig. 7 illustrates the V''_{DD} voltage level and the current mirror accuracy as a function of K. In fact, the voltage drop across transistor *P4* can be as little as 0.15 V when its *W/L* ratio is big enough to minimize its R_{ON} resistance. The lower graph of Fig. 7 shows that although V''_{DD} voltage levels close to V_{DD} can be achieved, the current mirror loses its accuracy when the V''_{DD} voltage level exceeds 4.75 V. This is due to the input voltage limitation of the operational amplifier OA2 which cannot approach the power supply rails. Therefore, to improve the accuracy of the current mirror, a rail-to-rail operational amplifier should be utilized.

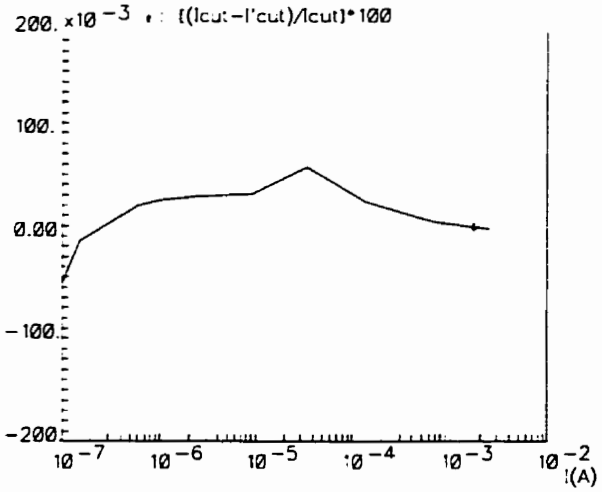


Fig. 6: The relationship between I_{CUT} and I'_{CUT} for different current levels.

For the applications that require supply voltage lower than 5 V, the proposed BICS provides a very good current sensing accuracy and the down converted voltage which

supplies the CUT remains stable and unaffected in both test and mission modes. Therefore, the BICS does not degrade the speed performance of the CUT. Furthermore, as all partitioned parts of the chip receive very close supply voltages in all conditions due to the existence of voltage regulators, the probability of latch-up, which is triggered due to unequal V_{DD}s or *GND*s on the same chip as explained in [8], is greatly reduced.

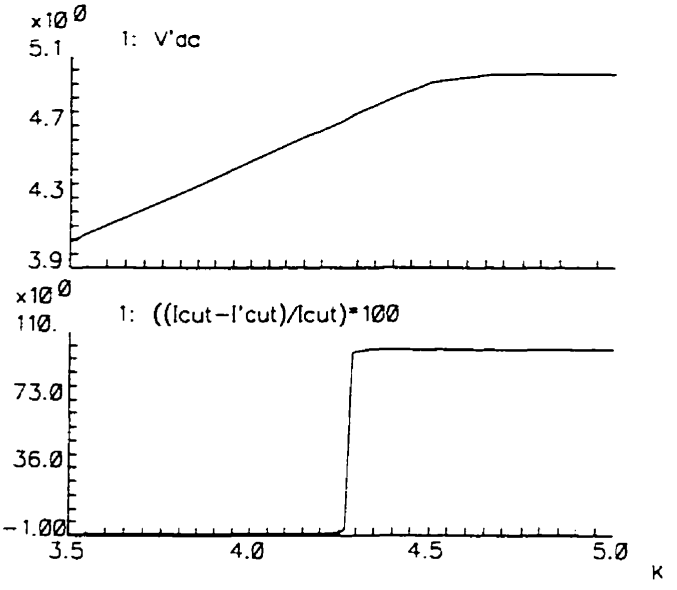


Fig. 7: V'_{DD}, I_{CUT} and I'_{CUT} versus $K = R_{P4}/R_{P5}$.

A simple circuit model similar to that used in [9] has been developed as the test vehicle. As shown in Fig. 8, it is composed of a series of n cascoded inverters driven by a stimulus and a fault injection circuitry. To adjust the magnitude of the static and transient currents, the *W/L* ratio of the transistors can be modified. The duration of the steady state and transient states is controlled by the frequency of the input stimulus and the number n respectively. The switch controlled by V_{fault} is closed to place the resistance R_{short} between V'_{DD} and *GND* in order to inject a fault. The R_{short} is adjusted to model various degrees of bridging faults.

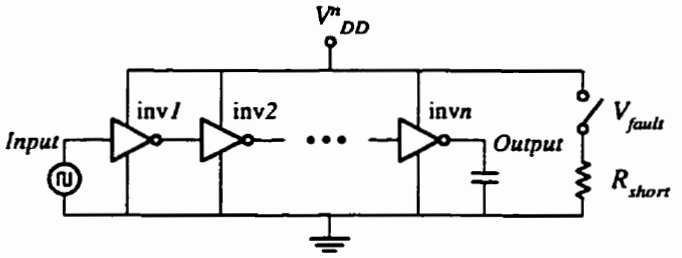


Fig. 8: The CUT model and fault injection mechanism.

Fig. 9 shows the input voltage, output voltage and the mirrored current of the CUT without fault. The effect of fault injection is shown in Fig. 10. It should be noted that the fault is injected periodically by the signal V_{fault}. In this experiment, W_n/L_n = 50/1, W_p/L_p = 100/1, and n = 20 which results in I_{DDQ} = 50 pA – 45 μA and the transient current of $I_{DD}(t)$ = 1.2 mA ~ 2 mA.

3 Power Dissipation Measurement

This current sensor does not require to be switched to measure the current and therefore can be used for on-line monitoring of the supply current of the circuit under test. The supply current can be used to measure the power dissipation of the circuit under test without interrupting it. Continuous power consumption verification would be useful to detect excessive power dissipation, which eventually causes chip deterioration. Power dissipation monitoring is also required to estimate the battery life-time of portable electronic systems. The proposed scheme to measure the average power dissipation P_{avg} consists of passing the transient current sensed through a grounded capacitor. At the beginning of the clock cycle the capacitor is instantaneously short circuited to initialize its voltage and then the voltage across the capacitor is held at the end of the clock period T ($V_{C_m}(T)$).

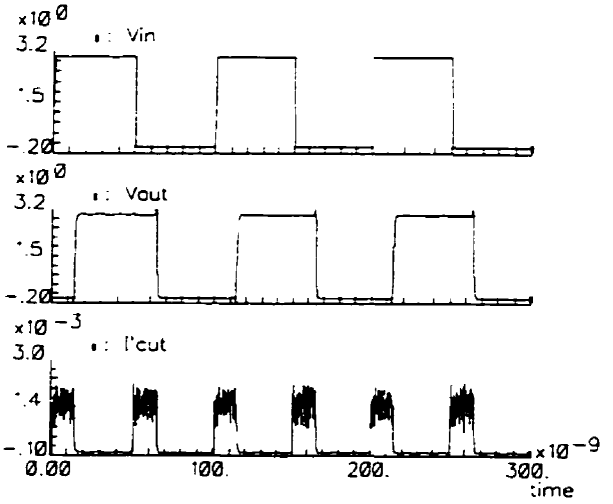


Fig. 9: The output currents without fault.

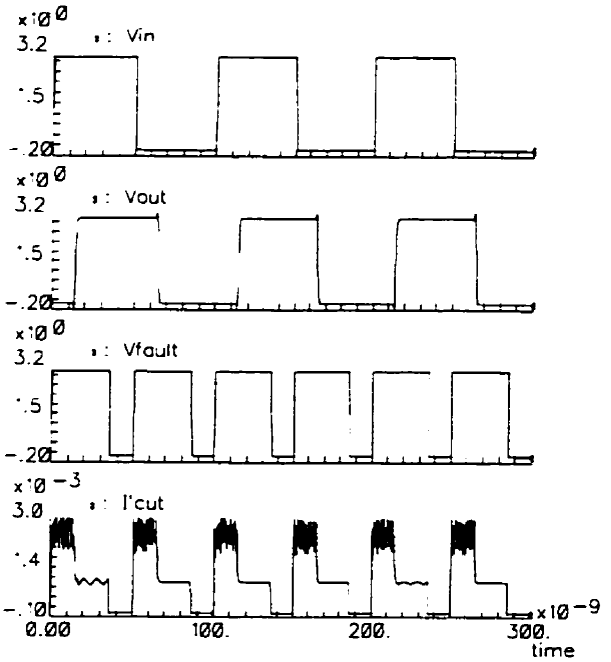


Fig. 10: The output currents in the presence of fault (R_{short} = 3 KΩ).

$$P_{avg} = \frac{1}{T}\int_0^T p(t)dt = \frac{V_{DD}}{T}\int_0^T I_{DD}(t)dt \qquad (6)$$

The voltage-current relationship of the capacitor is given by

$$V_{C_m}(T) = \frac{1}{C_m}\int_0^T I'_{DD}(t)dt = \frac{1}{NC_m}\int_0^T I_{DD}(t)dt \tag{7}$$

where N is the scale factor between I_{CUT} and I'_{CUT}. This suggest that

$$P_{avg} = \frac{V_{DD}}{T} NC_m V_{C_m}(T) \tag{8}$$

Therefore, knowing V_{DD}, T, N, and C_m in advance and measuring $V_{C_m}(T)$, we can accurately deduct the power dissipation of the CUT. Fig. 11 illustrates the on-line measurement of the power dissipation for our CUT model. At the end of the clock cycle the V_{C_m} is first sampled and held, and then the C_m capacitor is discharged by activating the signal *RST*.

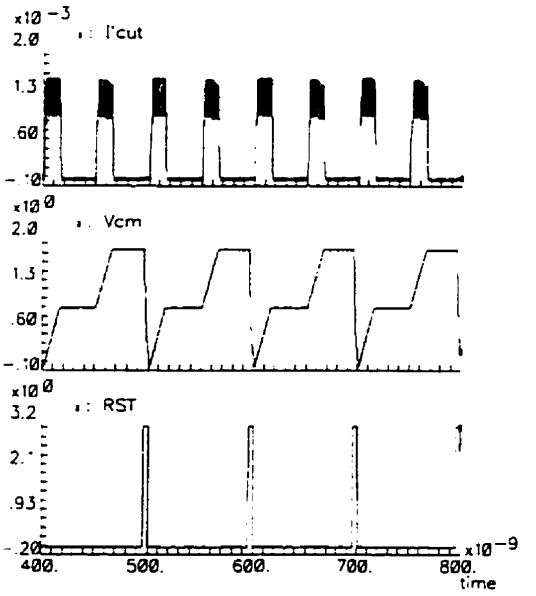


Fig. 11: Power dissipation measurement of the CUT model at each clock cycle

4 Measurement Element Design

As the result of the power dissipation measurement procedure is a voltage, we first convert the current sensed during I_{DDQ} testing procedure to a voltage using a resistor to

make these two procedures compatible. The resulting voltages from both cases are normally compared with a threshold value to verify whether the CUT pass the test or not. However, for the power dissipation measurement it is more interesting to measure the actual power dissipation of the CUT. Measuring the I_{DDQ} current level instead of comparing it with a fixed threshold voltage would also result in more accurate I_{DDQ} testing especially for mixed-signal circuits.

If the measurement ability is required, we propose to convert the voltage sensed to frequency using a voltage-controlled oscillator and then analyze the frequency on-chip. The oscillation frequency is a digital signal and can be analyzed using pure digital circuitry [15],[16]. The voltage to frequency converter can be used for both I_{DDQ} testing and power dissipation measurement.

Fig. 12 illustrates the schematic of the ME. The signal $\overline{CT} / PM$ sets the device in I_{DDQ} testing or power dissipation measurement mode. During I_{DDQ} testing, the resistor R_m is used to convert the current sensed to a voltage and the capacitor C_m is used to calculate the integral of the transient current in the power dissipation measurement mode. The capacitor C_m is reinitialized to zero using the signal RST before starting the power dissipation measurement.

The conversion to frequency of the resulting voltage is controlled using the $S / \overline{H}$ signal at the end of the clock period. The voltage across the resistor R_m during I_{DDQ} testing, or the capacitor C_m during power dissipation measurement, is sampled by the gate-source capacitance C_{gs} of the voltage-controlled oscillator's input transistor when the switch $S / \overline{H}$ is closed. This voltage is held in the capacitor C_{gs} and converted to frequency when the switch $S / \overline{H}$ is open. As shown in Fig. 12, the voltage-controlled oscillator is implemented as a simple current-controlled ring oscillator. The oscillation

frequency is determined by the delay time of each inverter and the number of inverters in the loop. The delay time of each inverter is determined by the amount of current supply through the current source, the input capacitance, the threshold of the inverter. The oscillator loop is composed of five inverters which establish a very high closed-loop gain to guarantee an instantaneous oscillation start-up. The proposed current sensor along with the voltage regulator and the ME have been designed and evaluated in CMOS 1.2 μm technology.

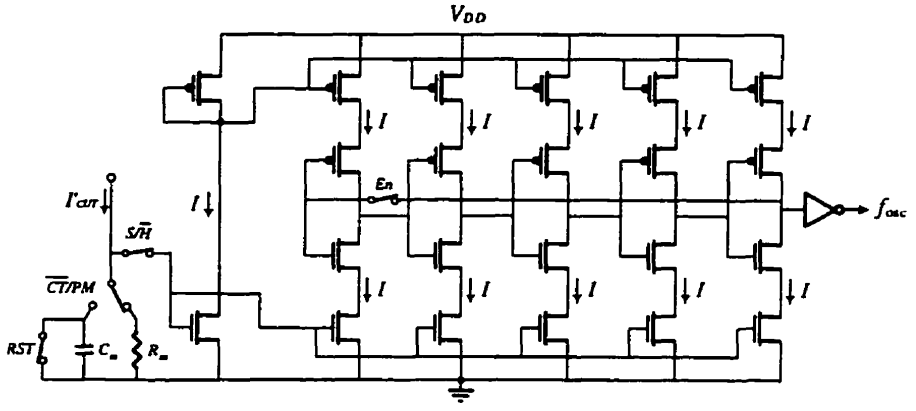


Fig. 12: Schematic diagram of the ME (*CT*: Quiescent Current Testing, *PM*: Power Dissipation Measurement).

5 Practical Considerations and Physical Implementation

In this section practical considerations necessary for successful insertion of BICSs as well as the result of physical realization are presented.

5.1 CUT Partitioning

Before proceeding to the implementation of BICSs in a VLSI circuit, the CUT should be partitioned into appropriate subblocks (SBs). Each SB should be independently supplied

through a dedicated BICS and therefore be separately tested. The size of SBs is determined by the upper limit of the I_{DDQ} level accepted for efficient fault detection. This approach allows to detect multiple faults if they occur in different SBs. Furthermore, as faulty SBs can be easily identified, fault diagnosis at SB level is achieved.

It should be noted that functional building blocks such as analog circuitry and on-chip oscillators that have relatively big static bias currents must not be placed in the same SB with digital circuitry. These building blocks increase considerably the I_{DDQ} level and make it very difficult to distinguish between faulty and normal static current levels.

5.2 Testability of the BICS

It is also of great importance to insure the complete functionality of the BICS itself before commencing the CUT verification. This should be performed in a self-test phase. Two main functions should be tested: the accuracy of the voltage down converter represented by V_{DD}^{n} and the accuracy of the current mirror characterized by its scale factor N ($I'_{CUT} = NI_{CUT}$). In the self-test phase, the CUT is replaced by a resistor R_{test} and the resulting current (V^{n}_{DD}/R_{test}) is mirrored and passed through the resistor R_m shown in Fig. 12. The voltage across the resistor R_m, given by the relationship (9), is then converted to a frequency to evaluate the result of the self-test.

$$V_{R_m} = NV_{DD}^{n}\left(\frac{R_{mt}}{R_{test}}\right) \tag{9}$$

Generally, the ratio of two resistors is very precise and therefore the tolerance of R_m and R_{test} will not affect the self-test phase. As the oscillation frequency is directly proportional to NV_{DD}^{n}, parametric deviation of N and V_{DD}^{n} can be detected. To eliminate the masking probability between N and V_{DD}^{n}, the accuracy of the current mirror can be

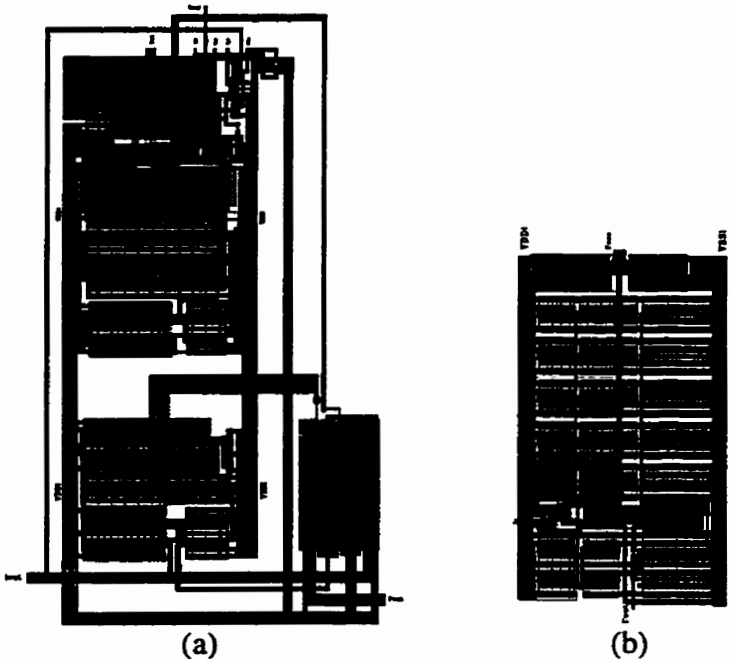
tested separately by replacing the CUT by a reference current I_{test}. In this case the voltage drop across the resistor R_m is given by

$$V_{R_m} = NR_{mt} I_{test} \tag{10}$$

By performing these self-test procedures, the functionality of the voltage down converter, the BICS and the current to frequency converter will be verified.

5.3 Physical Implementation

The presented BICS has been implemented using N-well CMOS 1.2 µm technology from MITEL Semiconductor. Fig. 13(a) depicts the layout of the BICS that occupies 0.13 mm^2. The current-to-frequency converter shown in Fig. 13(b), which can be common to all BICSs, occupies 0.027 mm^2 of active chip area. A microscope photograph of the fabricated chip is shown in Fig. 14.



(a) (b)

Fig. 13: Layout of different parts of the proposed BICS.

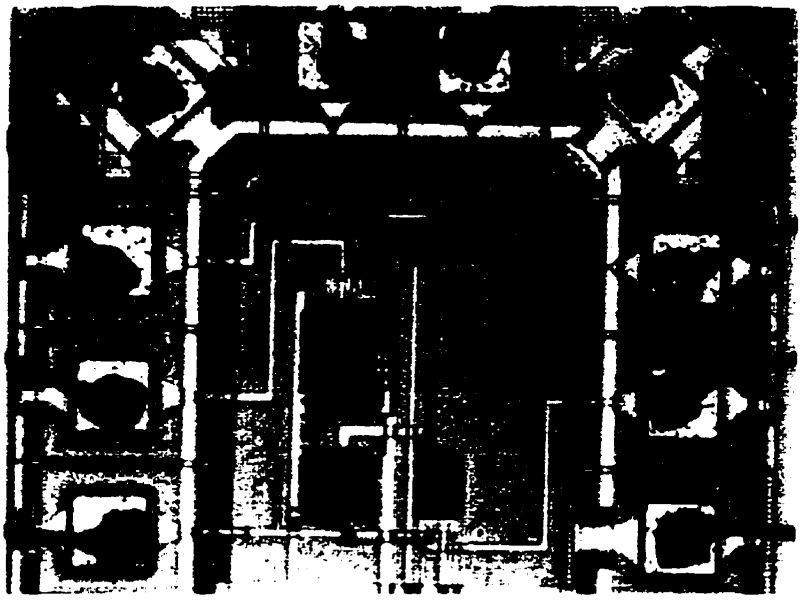


Fig. 14: Photograph of the fabricated chip containing the proposed BICS.

6 Test Procedures Summary

The presented BICS is used for both I_{DDQ} testing and power dissipation measurement. Before commencing the test procedure, a self-test phase should be performed to verify the functionality of the voltage reference generator, voltage adapter, and the BICS. The summary of different test phases is as follows.

6.1 Self-Test Phase

1) CUT is disconnected from the BICS and replaced by the resistor R_{test} and the oscillation frequency is evaluated. The precision of the voltage reference generator,

voltage adapter, and voltage regulator represented by V_{DD}^{n}, as well as the accuracy of the current mirror represented by N, are verified.

2) CUT is disconnected from the BICS and replaced by the current reference I_{test} and the output oscillation frequency is evaluated. Therefore, the accuracy of the current mirror is tested separately to eliminate the masking probability between N and V_{DD}^{n}.

6.2 I_{DDQ} Testing Phase

1) The signal $\overline{CT}$ / PM is set to zero to select the resistor R_m.
2) The test vector is applied and at the end of the clock cycle the signal S / $\overline{H}$ is activated to copy the voltage across the resistor R_m to the voltage to frequency converter's input.
3) The oscillation frequency is checked to evaluate the I_{DDQ} level.

6.3 Power Dissipation Measurement Phase

1) The signal $\overline{CT}$ / PM is set to one to select the capacitor C_m.
2) At the end of the clock cycle the signal S / $\overline{H}$ is activated to copy the voltage across the capacitor C_m to the voltage to frequency converter's input and then the capacitor is discharged by activation the signal *RST*.
3) The oscillation frequency is evaluated to measure the value of power dissipation.

7 Conclusion

A practical and accurate BICS for I_{DDQ} testing and on-line power dissipation measurement is proposed in this paper. It can be used to increase the test accuracy of off-chip tests and for full BIST solution based on I_{DDQ} monitoring. To the authors knowledge, no built-in

on-line power dissipation measurement technique has previously been reported in literature. The BICS presented can be used for a wide range of applications and technologies. It is most suitable for the applications that require on-chip supply voltage down-conversion. In this case, the BICS will not affect the CUT supply voltage level nor its speed performance. The BICS is easy to implement using small area overhead and can be used for current monitoring concurrently with the normal operation of the CUT. The BICS can be easily applied to multiple chip modules (MCM) by integrating the current sensor and the MCM on the same substrate. The basic principle of the proposed BICS for I_{DDQ} testing and on-line power dissipation measurement has been verified using a chip fabricated in CMOS 1.2 μm technology of MITEL Semiconductor. The experimental results confirm the accuracy of the proposed BICS.

References

[1] Rubio, A., J. Figueras, and J. Segura, "Quiescent Current Sensor Circuits in Digital VLSI CMOS Testing," *Electronic Letters*, 1990, vol. 26, no. 15.

[2] Nigh, P., and W. Maly, "Test Generation for Current Testing," *IEEE Design & Test of Computers*, 1990, vol. 7, no. 2, pp. 26-38.

[3] Agrawal, V.D., "Special Issue on I_{DDQ} Testing," *Journal of Electronic Testing, Theory and Applications*, 1992, Vol. 3.

[4] Soden, Jerry M., and Charles F. Hawkins, "I_{DDQ} Testing: Issues Present and Future," *IEEE Design & Test of Computers*, Winter 1996, pp. 61-65.

[5] Wallquist, Kenneth M., "On the Effect of I_{SSQ} Testing in Reducing Early Failure Rate," Proc. of the *IEEE Int'l Test Conf.*, 1995, pp. 910-914.

[6] *The National Technology Road Map for Semiconductors*, Semiconductor Industry association, San Jose, Calif. 1994.

[7] Nicolaidis, M., F. Vargas, and B. Courtois, "Design of BISCs for Concurrent Checking in Radiation Environments," *IEEE Trans. on Nuclear Science*, 1993, vol. 40, no. 6, pp. 1584-1590.

[8] Maly, W., and M. Patyra, "Built-In Current Testing," *IEEE Journal of Solid-State Circuits*, 1992, vol. 27, no. 3, pp. 425-429.

[9] Tang, Jing-Jou, Kuen-Jong Lee, and Bin-Da Liu, "A Practical Current Sensing Technique for I_{DDQ} Testing," *IEEE Trans. on VLSI Sys.*, 1995, vol. 3, no. 2, pp. 302-310.

[10] Shen, Tung-Li, James C. Daly, and Jien-Chung Lo, "A 2-ns Detecting Time, 2-μm CMOS Built-In Current Sensing Circuit," *IEEE Journal of Solid-State Circuits*, 1993, vol. 28, no. 1, pp. 72-77.

[11] Miura, Yukiya, and Kozo Kinoshita, "Circuit Design for Built-In Current Testing," Proc. of the *IEEE Int'l Test Conf.*, 1992, pp. 873-881.

[12] Hwang, Changku, Mohammed Ismail, and Joanne E. DeGroat, "On-Chip I_{DDQ} Testability Schemes for Detecting Multiple Faults in CMOS ICs," *IEEE Journal of Solid-State Circuits*, 1996, vol. 31, no. 5, pp. 732-739.

[13] Yoo, H.-J., *et al.*, "A Precision CMOS Voltage Reference with Enhancement Stability for the Application to Advanced VLSI's," Proc. of the *IEEE ISCAS*, 1993, pp. 1318-1321.

[14] Jolly, R.D., and R.H. McCharles, "A Low-Noise Amplifier for Switched Capacitor Filters," *IEEE Journal of Solid-State Circuits*, 1982, vol. SC-17, no. 6, pp. 1192-1194.

[15] Arabi, K., and B. Kaminska, "Built-In Temperature Sensors for On-line Thermal Monitoring of Microelectronic Structures," To be appeared in *Journal of Electronic Testing, Theory and Applications.*

[16] Arabi, K., and B. Kaminska, "Oscillation-Test Strategy for Analog and Mixed-Signal Integrated Circuits," Proc. of the *IEEE VLSI Test Symp.*, 1996, Princeton, pp. 476-482.

CHAPITRE 3

CONCEPTION POUR LA TESTABILITÉ DE LA PARTIE ANALOGIQUE DES CIRCUITS IMPLANTABLES

3.1 Résumé

Le développement de technologie d'intégration des circuits microélectroniques a donné la possibilité de concevoir des circuits électroniques VLSI. La probabilité d'avoir un circuit défectueux s'accroît avec le niveau d'intégration du circuit. La complexité et la densité d'une puce VLSI augmentent donc la probabilité que cette dernière soit défectueuse. L'adoption d'une stratégie de test au début de la conception s'avère être une étape importante dans le développement d'un circuit intégré. Comme il a été expliqué dans le chapitre précédent, plusieurs techniques efficaces et pratiques ont été développées pour améliorer le test des circuits numériques. Toutefois, moins d'attention a été accordé aux circuits analogiques et mixtes au niveau du test.

Le test des circuits analogiques et mixtes est plus compliqué que celui des circuits numériques à cause des facteurs suivants:

1) Les circuits analogiques sont caractérisés par plusieurs paramètres de nature différente comme le gain, la phase, la fréquence de coupure, la bande-passante, le taux de changement de sortie, l'impédance d'entrée, l'impédance de sortie, etc.

De plus, le nombre et la nature de ces paramètres changent d'un circuit à l'autre. Alors, dans la phase de test, il est très long et difficile de vérifier tous les paramètres du circuit, le test requiert des équipements dédiés au circuit sous test.

2) Le test des circuits analogiques est en général imprécis. Cette imprécision provient de: l'imprécision des appareils de génération des vecteurs de test, la tolérance du circuit sous test et l'imprécision du circuit évaluant la réponse du circuit sous test au vecteur de test appliqué. C'est pourquoi il faut élargir la marge de la bande de décision pour chaque paramètre. La marge de tolérance de chaque paramètre pour le circuit sous test doit être plus grande que celle définie par le concepteur lors du design du circuit. Cet élargissement de la bande de tolérance diminue la couverture de pannes.

3) Les circuits analogiques comportent plus de redondance que les circuits numérique. Ces redondances sont utiles pour stabiliser les caractéristiques du circuit, mais elles diminuent la couverture de panne dans la phase de test. Un exemple typique est un amplificateur opérationnel avec un gain en boucle ouverte très grand, qui est utilisé comme un amplificateur à gain limité en utilisant une boucle de rétroaction.

4) Les spécifications des circuits analogiques changent avec la fréquence d'opération. Il est alors obligatoire de vérifier la fonctionnalité des circuits analogiques à la fréquence d'opération du circuit.

5) Le manque d'un modèle de défauts puissant et pratique comme le modèle collé à 0/1 qui est très répandu dans le domaine du test numérique.

Plusieurs applications telles les télécommunications, l'automatique, l'instrumentation biomédicale, etc., nécessitent l'implantation de systèmes VLSI mixtes qui sont constitués de circuits analogiques et numériques dans la même puce. La partie analogique occupe seulement 20% à 30% de la surface active de la puce. Cependant, la majorité du temps de test et de conception des circuits mixtes est consacrée principalement à la partie analogique, due à la complexité naturelle des circuits analogiques.

Les chercheurs dans les milieux universitaires et industriels ont commencé à développer des approches qui couvrent la testabilité dans les circuits analogiques et mixtes, en y incluant la conception pour la testabilité et l'autovérification intégrée. Ces développements ont pour objectif de diminuer le coût de test et d'augmenter la fiabilité du produit final.

Le manque de méthodes efficaces et simples pour la conception pour la testabilité et l'autovérification intégrée des circuits analogiques et mixtes d'une part et le fait que tous les systèmes biomédicaux sont réalisés en utilisant de circuits mixtes d'autre part, nous ont encouragé à consacrer une partie importante de cette thèse à développer des techniques de test pour les circuits analogiques et mixtes. Les blocs analogiques le plus souvent rencontrés dans les systèmes biomédicaux sont les convertisseurs analogiques/numériques et numériques/analogiques, les filtres analogiques et les amplificateurs opérationnels. Vu la difficulté de test des convertisseurs de données, une attention particulière a été consacrée à leurs problèmes de test.

Les détails des techniques développées au cours ce cette recherche sont présentés dans les sections suivantes sous forme d'article scientifiques.

3.2 "BIST for Digital-to-Analog and Analog-to-Digital Converters"

Dans cette section, des approches efficaces pour l'autovérification intégrée des convertisseurs analogiques/numériques et numériques/analogiques seront introduites. D'abord, une technique d'autovérification intégrée a été développée pour les convertisseurs numériques/analogiques basée sur la mesure des paramètres statiques du convertisseur sous test. La même technique a été utilisée pour tester des convertisseurs analogiques/numériques qui utilisent un convertisseur numérique/analogique dans leurs structures.

Les avantages majeurs de ces approches sont une petite surface additionnelle et un minimum d'influence sur les performances du circuit sous test dus à la présence des circuits de test. Ce travail est paru dans la revue *IEEE Design & Test of Computers, Winter 1996, Vol. 13, No. 4, pp. 40-49.*

BIST for Digital-to-Analog and Analog-to-Digital Converters

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Abstract

A novel test approach and circuitry suitable for built-in self-test (BIST) of digital-to-analog (D/A) and analog-to-digital (A/D) converters using static parameters are proposed. Offset, gain, integral nonlinearity (INL), differential nonlinearity (DNL) and monotonicity are tested without using test equipment. An off-line calibrating technique has been used to insure the accuracy of BIST circuitry and to reduce area overhead by avoiding the use of high quality analog blocks. The proposed BIST structure presents a compromise between area overhead, test time and test coverage. By only a minor modification the test structure would be able to localize the fail situation and to test all D/A converters on the same chip. The BIST circuitry has been designed and evaluated using CMOS 1.2 μm technology. The simulation results show that assuming the BIST voltage references fulfill the required accuracy, the BIST structure is applicable for testing D/A and A/D converters

up to 16-bits of resolution. The small value of area overhead, the simplicity and efficiency of the proposed BIST architectures seem to be promising for manufacturing.

1 Introduction

The development of CMOS and BiCMOS technologies has made it possible to combine digital and analog circuits in a single chip and offers the possibility of designing high quality analog circuits [1]. In the manufacturing of monolithic mixed-signal integrated circuits, industry has found that two factors dominates production costs. These are the direct costs of test equipment and test time; and the indirect costs of test procedure development [2],[3].

We can assume that effective methods for testing the digital circuitry are known, but testing the analog circuitry is still a problem. Researchers have devoted much efforts to testing pure analog circuits and designing testable analog and mixed circuits [4]-[7]. Until recently, however, they have not arrived at a general and efficient solution. Two approaches have emerged, each with a different influence on the internal structure of the device to be tested. One tests an isolated integrated circuit using of specialized testing equipment. This approach, which employs design-for-testability techniques, emphasizes the aspects of controllability and observability that require access to the internal test points. Choosing a suitable form of excitation signals and methods of evaluation of the output signals are separate problems.

The second approach tests an integrated circuit within its environment and requires built-in self-test (BIST) capabilities. Measurement and control circuits must reside on the same chip and should be able to present the binary pass/fail result.

The most frequently encountered parts of mixed digital and analog circuits are digital-to-analog (D/A) and analog-to-digital (A/D) converters, which bridge the gap between digital and analog systems. Although many publications cover the design, specification and applications of D/A and A/D converters, few articles discuss testing conversion products that need expensive mixed-signal test equipment [8],[9]. Appropriate BIST methods, however, can eliminate the need for such test equipment [2].

A/D converters have more complicated architectures than D/A converters, hence the area overhead related to BIST circuitry is not a critical problem. In contrast, the inherent simplicity of low-resolution D/A conversion process leads to relatively simple architectures, for which the area overhead of BIST can be a burden. It has been shown that a D/A converter with a resolution up to 10-bit can be obtained by standard methods. From design point of view, to obtain a higher resolution, calibration techniques are used that significantly increase the area of a D/A converter [1]. In this case, the area overhead of BIST can be very small compared to that of the D/A converter.

The specific BIST approach presented in [10] requires a D/A and an A/D converter on the same chip and uses an off-chip D/A converter and external logic test equipment. Conventional test techniques have been applied to embedded A/D converters using microcontroller resources available on the same chip [11],[12]. A digital BIST for a signal-to-noise-ratio test of an oversampled A/D converter, based on an available digital signal processing core, has been also presented in [3]. Its developers, however, did not report the related area overhead.

In this paper, we propose a practical BIST approach to automatically test the offset voltage (V_{OSE}), differential nonlinearity (DNL), integral nonlinearity (INL) and gain error (G_{FSE}) of medium to high-resolution D/A converters without using mixed-mode or logic

test equipment. Then, we map the same technique to test a wide range of A/D converters. The proposed BIST structures do not require microcontrollers or digital signal processing cores on the chip.

The paper is organized as follows. Section II discusses the basic characteristics of data converters. Section III presents the proposed BIST architecture and test procedure for the functional testing of D/A converters. A new test approach dedicated to A/D converters, having a D/A converter in their architecture, is introduced in section IV. Section V discusses the design and implementation of the main system blocks. A summary of BIST results is presented in section VI.

2 Basic Characteristics of D/A and A/D Converters

In general, D/A converter is considered at system level where both analog and discrete state behaviors are present. The inputs to a D/A converter are N-bit digital words b_1b_2 ... b_N and a reference voltage (V_{REF}). The output voltage of a D/A converter can be expressed as:

$$V_O = V_{REF}(b_1 2^{-1} + b_2 2^{-2} + ... + b_N 2^{-N}) \quad (1)$$

Testing offset, integral nonlinearity, differential nonlinearity and gain error can verify the functionality of a D/A converter. Integral nonlinearity, ε_i, is the (peak) deviation of a data converter transfer characteristic from an ideal or best straight line with offset and gain errors zeroed. Differential nonlinearity, $\varepsilon_{i,i-1}$, measures the separation between adjacent levels. Differential nonlinearity error is an important parameter for many applications that require uniform spacing of the output voltages of the D/A converter [13].

We specify ε_i and $\varepsilon_{i,i-1}$ as fractions of the least significant bit (LSB) (less than 1/2 LSB and greater than -1/2 LSB). Fig. 1(a) shows the ideal static behavior of a D/A

converter and the relationship between ε_i, ε_{i-1} and $\varepsilon_{i,i-1}$. Fig. 1(b) clarifies the definitions of DNL, INL, V_{OSE}, G_{FSE}, and monotonicity. The D/A converter characteristics presented in this section are also applicable to an A/D converter by just interchanging the input and output definitions.

Static testing is a slow operation and requires a much longer time for each test step than the settling time of the D/A converter under test. When superposition error (bit interaction) is less than 1/10 LSB, it is possible to shorten the test procedure and test individual bits. A low value of this error allows the integral linearity error at any binary word to have the same magnitude (with the opposite sign) as the one's complement of that code [13]. Bit interaction greater than 1/10 LSB occurs frequently in high-resolution D/A converters.

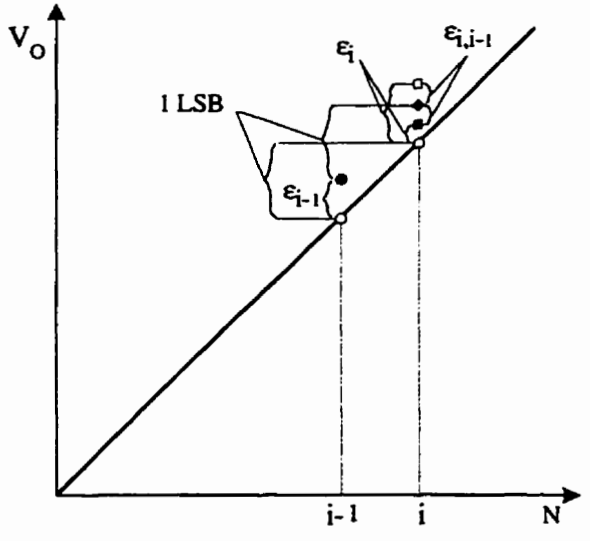

Fig. 1(a): Ideal static behavior of a D/A converter and the relationship between ε_i, ε_{i-1} and $\varepsilon_{i,i-1}$. (N: input digital word, V_O: analog output voltage, •: output voltage at i-1, ◻ or ▪: output voltage at i, o: expected ideal output voltage (INL error is zero) at i and i-1, and ◆: expected output voltage at i if DNL error is zero based on the output voltage (denoted by •) at i-1.

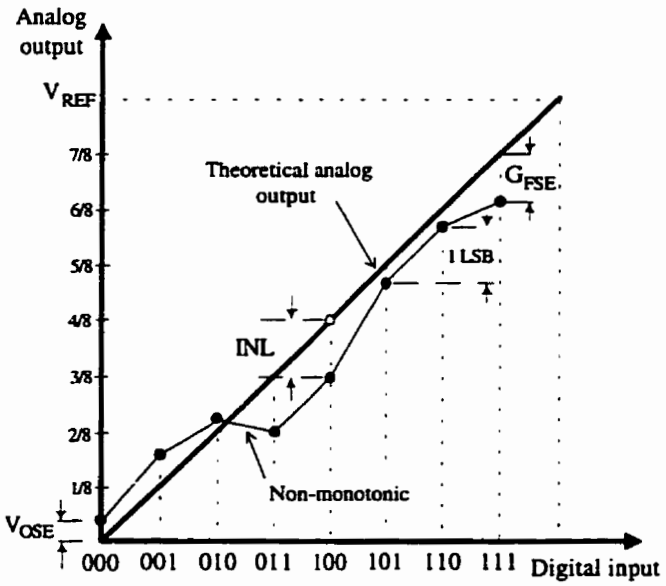

Fig. 1(b): Graphical representation of INL, V_{OSE}, G_{FSE}, and nonmonotonicity for a 3-bit D/A converter.

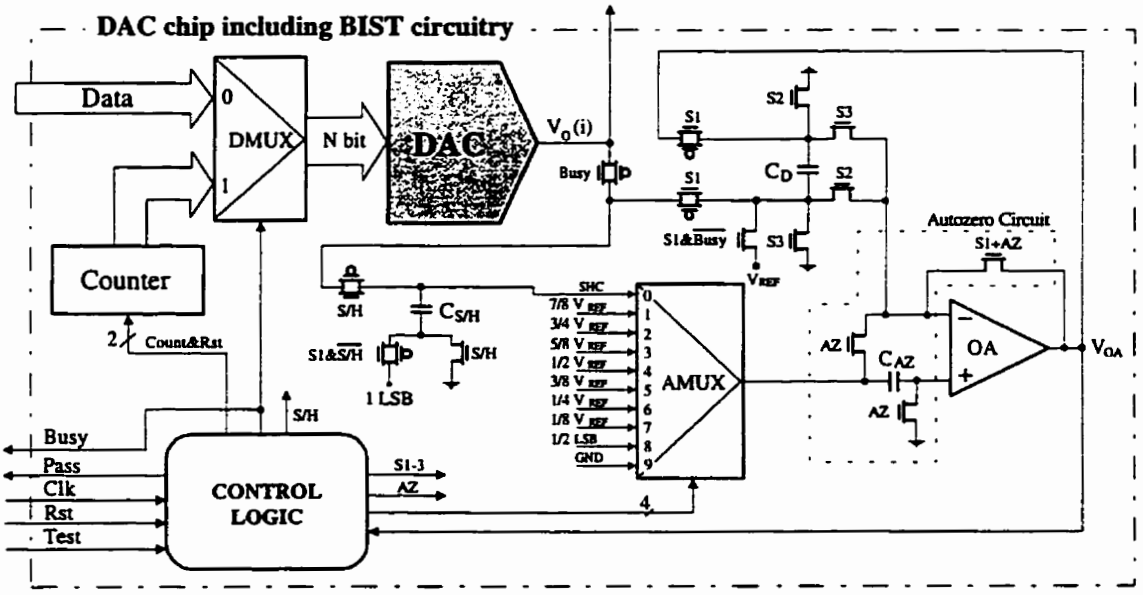

Fig. 2: BIST architecture for D/A converter testing.

Since the BIST approach presented in this paper is intended for low to high-resolution D/A converters, all 2^N possible input test vectors are applied for DNL testing but INL is tested at some critical points of operation.

3 Functional Testing of D/A Converters

3.1 Introduction

The performance degradation and area overhead of the test structure's presence are the most essential problems in analog BIST approaches. In order to reduce the area overhead, the proposed BIST structure does not use a reference D/A converter that normally has 3 to 4 more bits of resolution, as in previous works [9],[13]. The BIST architecture generates the input stimulus and evaluates the output response without using external equipment. This reduces test time, because we neither calibrate external equipment nor calculate parameters by a processor. In this section the new BIST architecture and test algorithm are presented.

3.2 BIST Architecture for D/A Converter Testing

Fig. 2 illustrates the proposed approach for testing some static characteristics of D/A converters in order to verify their functionality. This BIST approach can be applied to every type of D/A converter.

The test architecture shown in Fig. 2 consists of six main parts.

1) An *N*-bit counter which produces the input test vectors.
2) A digital multiplexer (DMUX) which selects the *N*-bit counter output or functional data.

3) An analog multiplexer (AMUX), switches and test voltage references which make the BIST structure programmable.
4) An operational amplifier (OA) which acts as part of comparator, voltage references and sample-and-hold (SHC) circuits at different times. It measures and evaluates the various parameters to be tested.
5) An autozero circuit, which uses a capacitance and two NMOS switches to store and then cancel the introduced offset voltages.
6) A control logic (CL), which directs the test procedure using a finite state machine (FSM).

When the *Test* input becomes active, the control logic begins the test procedure and directs the operation of the counter, D/A converter, analog switches and AMUX, and observes the comparator output.

This BIST structure tests V_{OSE}, differential nonlinearity (DNL), $\varepsilon_{i,i-1}$, (at all 2^N input codes), G_{FSE}, and integral nonlinearity (INL), ε_i, at 7/8 V_{REF}, 3/4 V_{REF}, 5/8 V_{REF}, 1/2 V_{REF}, 3/8 V_{REF}, 1/4 V_{REF}, and 1/8 V_{REF}. It computes these quantities using the following equations.

$$V_{OSE} = V_O(00...0) - GND \tag{2}$$

$$G_{FSE} = V_O(11...1) + 1\ LSB - V_{REF} \tag{3}$$

$$\varepsilon_{i,i-1} = V_O(i) - V_O(i-1) - 1\ LSB \tag{4}$$

$$\varepsilon_i = V_O(i) - (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3}) \times V_{REF} \tag{5}$$

where $i = b_1 b_2 b_3 ... b_N$, and b_1 is the most significant bit.

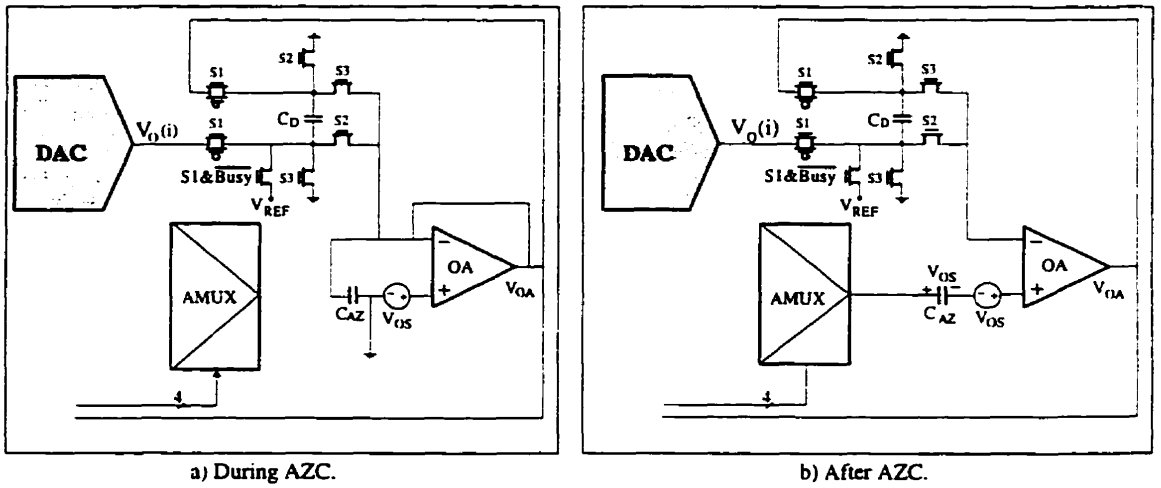

Fig. 3: Autozeroing of OA offset voltage.

The measured parameters are alternately compared with 1/2 LSB and -1/2 LSB values (or maximum acceptable-tolerance margin defined by the designer) to verify that they are within the maximum allowable error voltage. The procedure of measuring and evaluating the parameters are described in details in the test procedure section.

3.3 Autozeroing Technique

In order to provide the necessary accuracy for testing up to 16-bit D/A converter, it is important to remove the offset voltages that may be introduced by the OA and other parts of the BIST structure. In all test phases, the OA input offset is effectively zeroed during autozero cycle (AZC) by sampling and storing it in the C_{AZ}. The connections during and after AZC are shown in Fig. 3.

During the autozero cycle, AZ is active and AMUX selects GND, thus the OA is connected in the unity gain configuration and the input offset is available at its output. Capacitor C_{AZ} stores the offset across its terminals. After applying the offset-cancellation

algorithm, C_{AZ} is placed in series with V_{OS} at the noninverting input of the OA to cancel the existing offset voltage. The idea of offset-cancellation offers the possibility of automatically canceling the offset voltage without using external pins.

3.4 Test Procedure

When the *Test* input becomes active, control logic performs a self testing to verify the test circuitry's functionality and then activates the *Busy* and *Pass* signals to 1 and 0. It then begins the D/A converter testing. A flow chart of the BIST is shown in Fig. 4. It explains the complete test algorithm, which consists of the following phases:

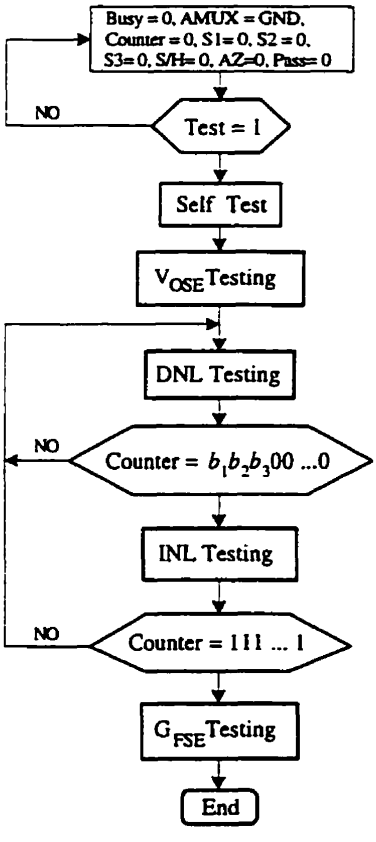

Fig. 4: Simplified flowchart of the BIST for D/A converter

Self-testing

Before beginning the data converter verification, it is necessary to ensure that the BIST structure is functional. In the first self-test cycle, signals S1, S/H and AZ are active and *Busy* is inactive, thus $C_{S/H}$ is charged to V_{REF}. In the second self-test cycle, *Busy* remains inactive, AMUX selects SHC and S1 becomes active, thus C_D is charged ideally to 1 LSB. Then AMUX selects ½ LSB, the S3 and S2 become alternately active resulting in the comparison between the C_D voltage and ±½ LSB. The output of the OA is verified by the CL and must be 1 and 0 consequently. This verifies the functionality of the test structure, except for the counter and DMUX, which a scan-based BIST technique can test. The self-test phase takes 4 clock cycles.

V_{OSE} Testing

In this phase, the counter is set to zero and autozero cycle is performed. In the second cycle AMUX selects GND and S1 becomes active therefore capacitor C_D is charged to the V_{OSE} (AZ=0). In the last two cycles of V_{OSE} testing, AMUX selects ½ LSB and S3 and S2 become active consequently resulting the V_{OSE} to be compared with ±½ LSB. In both cycles, the V_{OA} is verified by CL. This phase takes 4 clock cycles.

DNL, $\varepsilon_{i,i-1}$, Testing

During DNL testing the following operations are performed: V_O is held in the $C_{S/H}$ by activating S/H signal and the AZC is executed. Then the counter is incremented, AMUX selects the output of SHC and S1 becomes active. Therefore capacitor C_D is charged to the $\varepsilon_{i,i-1}$. In the last two cycles, AMUX selects ½ LSB and S3 and S2 are activated. In both cycles the V_{OA} is verified by CL, therefore V_{OSE} is compared with ±½ LSB. Fig. 5

shows the timing diagram of the test cycles during DNL testing. The DNL testing procedure takes 5 clock cycles for each input code, therefore the complete DNL testing time (T_{DNL}) is

$$T_{DNL} = 5 \times 2^N / f \tag{6}$$

where f is the test circuitry's clock frequency.

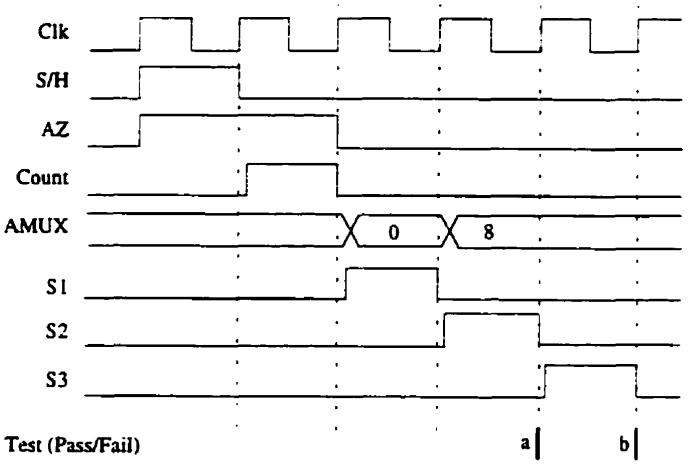

Fig. 5: Timing diagram of test cycles during DNL testing. During this phase *Busy* is set to 1 (a: V_{OA} is compared to ½ LSB and b: V_{OA} is compared to -½ LSB).

INL, ε_i, Testing

In the first clock cycle, counter is set to $b_1b_2b_300...0$ and AZC is performed. In the second clock cycle, AMUX selects $(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3}) \times V_{REF}$ and S1 becomes active, thus charging C_D to ε_i. In the last two cycles, ε_i is compared with ±½ LSB. In this phase, the deviation of the output voltage of the D/A converter from the ideal values corresponding to the three most significant bits is tested.

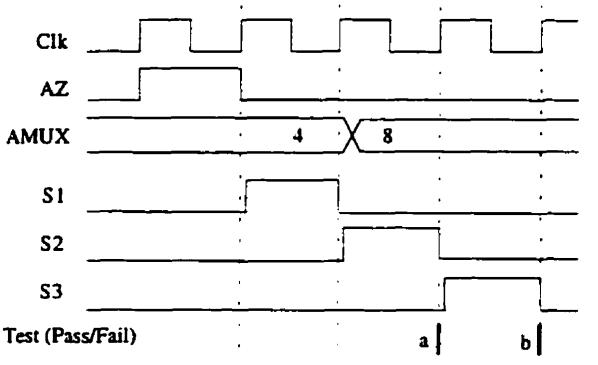

Fig. 6: Timing diagram of test cycles during INL testing. During this phase *Busy* is set to 1 (a: V_{OA} is compared to ½ LSB and b: V_{OA} is compared to -½ LSB). In this example i = 100 ... 0.

Each INL testing phase takes 4 clock cycles, and complete INL testing takes 28 clock cycles. Fig. 6 shows the timing diagram of the circuit during test for i = 1000...0. The $b_1b_2b_3$ value equal to 000 corresponds to V_{OSE} testing.

G_{FSE} Testing

The counter equals 11...1, AZC is accomplished and $V_O(i)$ is held in $C_{S/H}$ by activating S/H signal. Then, *Busy* signal becomes inactive, AMUX selects SHC, and S1 becomes active. This charges C_D to G_{FSE}. Finally, G_{FSE} is compared to ±½ LSB in the last two cycles. G_{FSE} testing takes 4 clock cycles.

As just explained, after each test phase, the measured parameters are alternately compared with +½ LSB and -½ LSB by means of the OA that has ½ LSB at its noninverting input and the C_D voltage or the inverse of C_D voltage at its inverting input. The OA output represents the test result that is observed by the CL. The proposed test set is capable of accurately testing the D/A converters with a resolution as high as 16 bits.

This structure exercises all 2^N codes measuring and evaluating V_{OSE}, G_{FSE}, $\varepsilon_{i,i-1}$, and ε_i (for the last three significant bits) in total time:

$$T_{TOTAL} = (40 + 5\times2^N)/f \tag{7}$$

where the clock frequency f is limited by the combined settling time of the D/A converter and the OA. We can assume that the complete test time approximately equals T_{DNL}.

3.5 Multiple D/A Converter Testing

Analog and mixed-signal application specific integrated circuits (ASIC), such as implantable multichannel microstimulators, normally contain more than one D/A converter in their architecture. As illustrated in Fig. 7, the presented BIST approach for D/A converter testing can be applied to test all available D/A converters on the chip that use the same reference voltage and have the same resolution. The implemented BIST circuitry selects one of the D/A converters each time and perform all test phases to verify its functionality. In this case, the area overhead is significantly reduced.

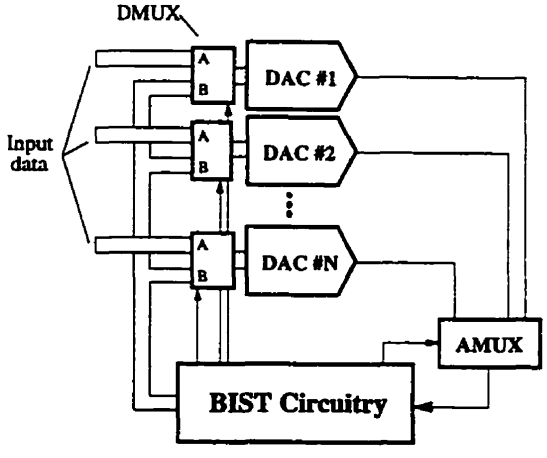

Fig. 7: Block diagram of multiple D/A converter testing.

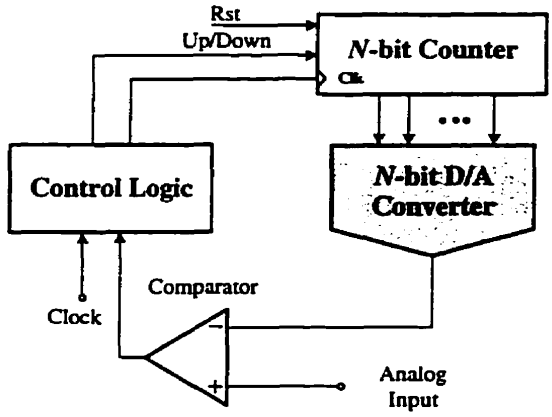

Fig. 8: Block diagram of staircase D/A converter.

4 BIST for A/D Converters

In an A/D converter, each digital output code corresponds to a continuous range of analog input values. Hence, the functional testing of A/D converters is more complex than for D/A converters and the related BIST architecture results in a higher area overhead.

A/D converters can be classified into three main categories: integrating, flash and those using D/A converters [14]. Designers often prefer the first category as the majority of the additional circuitry are digital and therefore easily implemented in CMOS technology. This category includes successive-approximation, staircase, pipeline, and subranging A/D converters.

In this section, we propose a new BIST approach for testing A/D converters based on the BIST technique explained earlier for D/A converter testing. The main idea is to rearrange the A/D converter architecture in the test mode and then to test its internal D/A converter using the developed BIST approach in this paper. This verifies the functionality of the remaining internal blocks of the A/D converter, because they all contribute to the D/A converter testing process. This approach is applicable to all A/D converters

employing D/A converters in their architecture. A Scan BIST technique can also be incorporated to test the digital section.

The A/D converter test approach has been applied to a staircase A/D converter. Fig. 8 shows the block diagrams of a staircase A/D converters which employs a D/A converter, a counter and a comparator in a feedback loop with control logic. Fig. 9 shows a BIST architecture for the staircase A/D converter. In the conversion mode the AMUX selects Analog input 10; *Busy* and other control signals are set to 0. Therefore, the test circuitry are disabled, the D/A converter output is connected to negative input of the comparator and D/A converter performs its normal function. This approach has several advantages.

First, its area overhead is very small, because the BIST architecture reuses the comparator and the counter already available in the A/D converter. The area overhead stems from analog switches, voltage references and a portion of control logic that occupy a very small area comparing with the A/D converter area. Therefore, the required BIST circuitry for A/D converter is much smaller than that for D/A converter. In general, the area overhead related to this technique amounts less than 5% of the total active chip area.

Functional testing an A/D converter is time consuming, because the input voltage must be slowly varied to find the transition voltages. The known methods to speed up the process of finding transition voltages, such as a computer-controlled D/A converter or a servo loop to automatically adjust the input voltage, are not appropriate for BIST. In our approach, as the same test procedure is performed for both data converters, the test time is the same for either D/A or A/D testing.

The possibility of testing the internal D/A is advantageous, because the A/D converter's precision depends directly on that of its D/A converter. If the D/A converter

that is used in an A/D converter is nonlinear, the step size will deviate from the ideal 1 LSB step size [13].

As a result, this method reduces the manufacturing cost by reducing the test cost. The integrating types and flash A/D converters can be tested by the reported approaches for analog and mixed signal testing [5],[7],[8]. These techniques, despite their efficiency for analog testing, are unsuitable for BIST in an A/D converter.

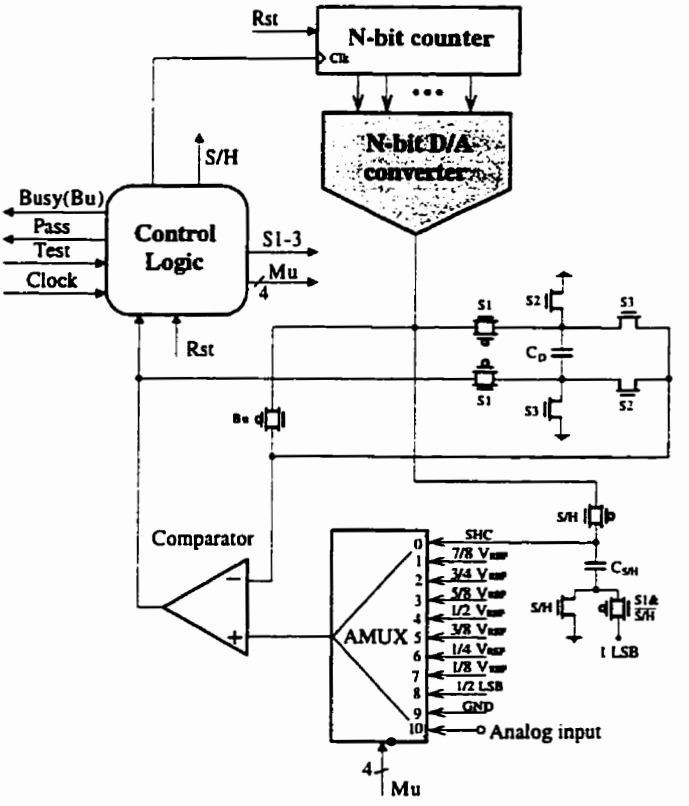

Fig. 9: The BIST architecture for structural testing of the staircase A/D converter.

5 BIST Design Features

In this section, the design considerations and operating features of the various subassemblies are discussed.

5.1 MOS Switches

The switches are the key components in analog testing and provide the test structure's programmability. The accuracy of the switches directly affects that of the test and therefore the functionality of the test system, especially when we are dealing with low voltage signals. Due to its non-ideal characteristics, it may causes serious performance degradation of the circuit under test. The most important characteristics of a switch are its on and off resistances (R_{ON} and R_{OFF}) and the values of its parasitic capacitors.

A simplified model of a non-ideal switch is presented in Fig. 10. Capacitors C_1, C_2 and C_{12} are the parasitic capacitors associated with switch terminals 1 and 2 and ground. Capacitors C_{1C} and C_{2C} are parasitic capacitors (the overlap capacitances) that may exist between the control voltage terminal C and the switch terminals 1 and 2.

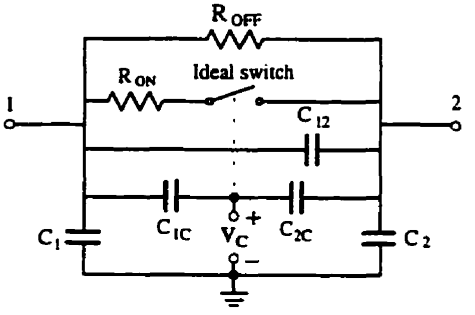

Fig. 10: Simplified model of a non-ideal switch.

The most serious limitations of a monolithic switch is the channel charge injection and the clock feedthrough [15] in which a portion of the control voltage appears at switch terminals 1 and 2 due to the existence of C_{1C} and C_{2C}. Using a CMOS switch, the feedthrough effects are diminished via cancellation and at the same time R_{ON} is reduced.

In order to reduce the channel charge injection and the clock feedthrough the following techniques are considered in the designing of the switching circuit:

1) The W/L ratio is chosen to be 4/2 μm to avoid short-channel effects and to minimize the parasitic capacitor values.

2) The switching circuit is designed to be symmetric. The switch charge injection and clock-feedthrough are canceled to the first order due to the balanced nature of the switching circuit. This means that, the error voltage introduced by each switch is compensated by another switch in the switching circuit.

Extensive simulations showed that the switching circuit ensures the required accuracy for our application. The symmetry of switching process in the measurement part of the BIST architecture minimized the error voltage introduced by parasitic capacitors.

5.2 Operational Amplifier

The OA contributes in many operations of the system. It is used as a part of the sample-and-hold circuitry, the voltage references and comparator block at different times. Very low offset voltage, low output impedance and high input impedance are therefore required. The OA's offset voltage is a critical parameter in our application and we sought to minimize it.

An unbuffered CMOS OA with n-channel input pair has been chosen to fulfill these requirements. A schematic diagram of the OA is shown in Fig. 11. During the simulation process, various devices were adjusted to achieve desired performance. The offset voltage has been reduced to less than 10 μV.

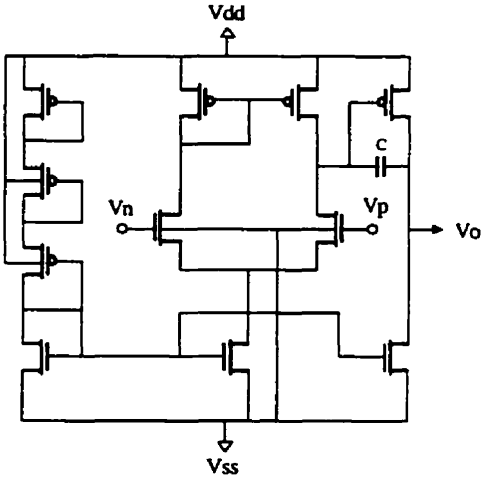

Fig. 11: Schematic of the CMOS operational amplifier.

5.3 Voltage References

High precision and stability are required for a voltage reference. In our case the implementation of the voltage references was not difficult to perform because the main reference voltage, V_{REF}, is already available on the chip. This assures the precision and stability of voltage references. A reference voltage is typically dependent upon the load connected to it. In order to maintain the precision of the reference, it is necessary to use a buffer amplifier to isolate the reference voltage from the load, and we have used the available OA to do so. We also used a dynamic element matching technique to increase the accuracy of voltage references up to 16 bit of resolution.

5.4 Control Logic

Control logic is a synchronous finite state machine which directs all the operations of the system. At the beginning of the test process, it performs a self-test in order to verify the functionality of the test structure. After self-testing, control logic carries out D/A

converter testing for all the 2^N input codes. The flowchart of the control logic is found in Fig. 4. Also with a minor modification of the control logic and by adding some output pins to the system, it would be possible to localize the fail situation.

6 BIST Results

By eliminating the test equipment the total test time by the BIST has been reduced to approximately $5\times2^N/f$ s (as explained earlier) for A/D and D/A converter testing, which is a significantly shorter test time than using external test equipment [9]. The BIST circuitry circuit was designed and evaluated using CMOS 1.2 μm technology. The proposed test structure was exhaustively simulated and evaluated for a 12-bit D/A converter by exercising all 2^N input codes under the Analog Artist® environment from Cadence. The introduced V_{OSE}, DNL, INL and gain errors (G_{FSE}) were fully detected by the implemented BIST.

Fig. 12 shows some simulation results reflecting faulty and correct operation of a 12-bit D/A converter with V_{REF} = 5 V. Fig. 12(a) and Fig. 12(b) present two samples of DNL testing for the D/A converter having no faults. The output voltage of the OA (V_{OA}) indicates the correct operation (pass). Fig. 12(c) and Fig. 12(d) correspond to DNL testing for the D/A converter under faulty condition. In this case, the V_{OA} value is around -5 V which indicates the presence of a fault. It should be noted that the V_{OA} is adjusted to digital levels before being fed to the CL.

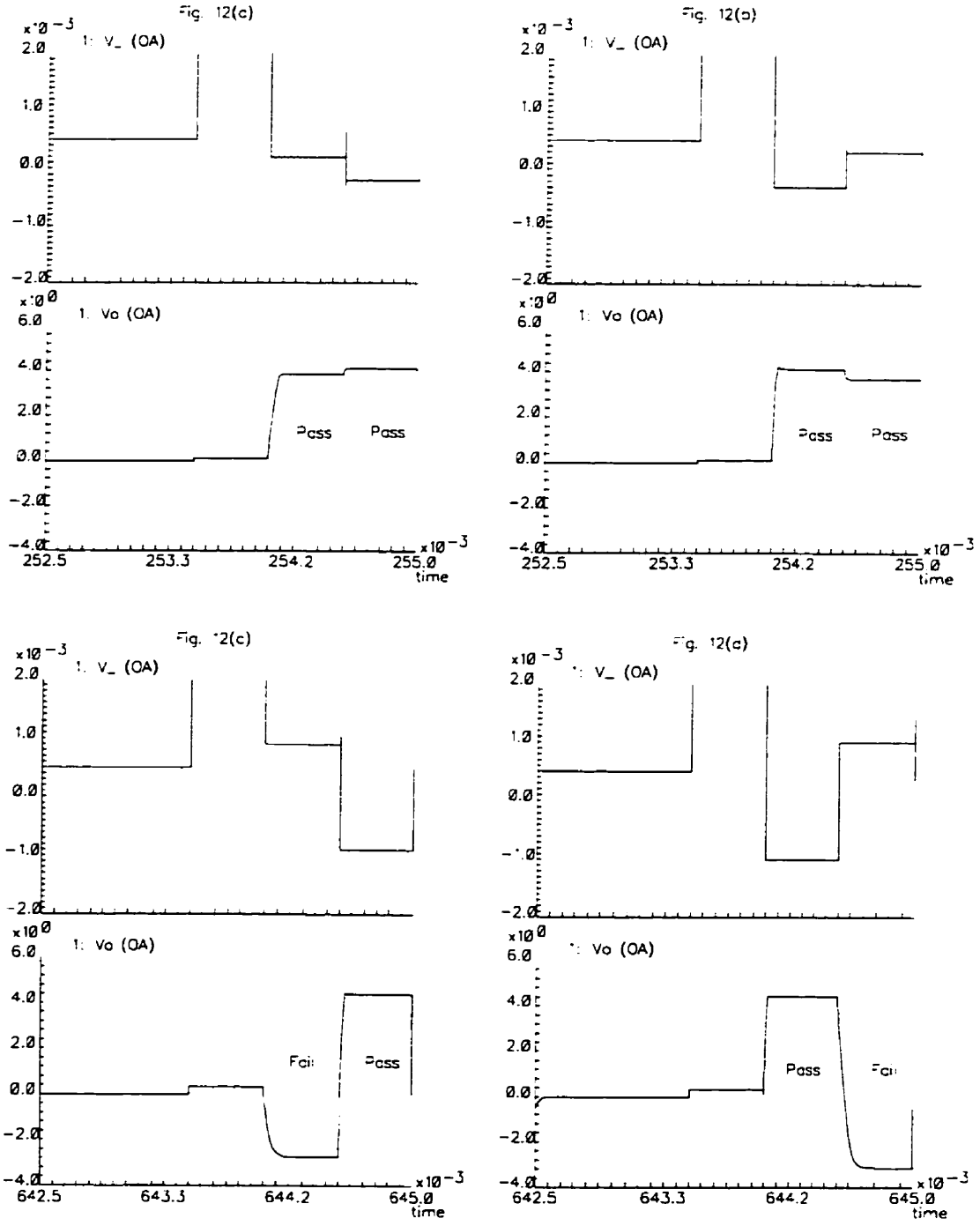

Fig. 12: Pass and fail situations for DNL testing of a 12-bit D/A converter for $V_O(i) \approx 122$ mV, $\varepsilon_{i,i-1} = 200$ μV (a); $V_O(i) \approx 122$ mV, $\varepsilon_{i,i-1} = -300$ μV (b); $V_O(i) \approx 312.5$ mV, $\varepsilon_{i,i-1} = -900$ μV (c); and $V_O(i) \approx 312.5$ mV, $\varepsilon_{i,i-1} = -1000$ μV (d). V_{REF} equals 5 V, and introduced comparator offset voltage V_{OS} is about 500 μV.

The simulations performed for 16-bit D/A converters demonstrated that the autozero technique and switching-circuit design ensure the required accuracy for high-resolution D/A converter testing. For these simulations, we assumed that the BIST voltage references have the required accuracy. In practice, however, it is difficult to generate voltage references with an accuracy of more than 16-bit on-chip. Therefore, the accuracy of the on-chip BIST voltage references limits the resolution of the BIST structure.

The area overhead related to the BIST structure, including digital and analog circuitry, based on the average area of medium to high-resolution D/A converters [1],[16]-[20], amounts to less than 5% of the total active chip area and it is less for A/D converters. These evaluations show that the presented BIST yields the same testability as conventional testing and applies to pass/fail D/A and A/D converter testing for manufacturing.

7 Conclusion

A practical BIST approach for the functional testing of D/A converters has been presented and evaluated. It can be applied to any type of D/A converters. An extension to A/D converter testing by applying the same BIST structure is also proposed. The BIST performs a self-test to verify its functionality and then begins D/A converter testing. The proposed BIST structure is optimized to reduce the area overhead, test time, performance degradation and to maximize the fault coverage. The obtained area overhead is very small and reasonable for mixed-circuit testing. The control logic can be eliminated if there is a microcontroller on the chip. The proposed BIST architecture is relatively simple and easy to realize.

These results show that our BIST design is applicable to the pass/fail testing of D/A converters and seems to be promising for manufacturing. Offset-cancellation by means of the autozero technique significantly improves the accuracy of the BIST structure. It allows to avoid implementing high quality analog building blocks. We hope that our BIST calibration technique encourage further research into the design of high-performance analog BIST circuitry.

References

[1] Wouter, D., *et al.*, "A Self-Calibration Technique for Monolithic High-Resolution D/A Converters," *IEEE J. Solid-State Circuits*, Vol. 24, No. 6, Dec. 1989, pp. 1517-1522.

[2] Arabi, K., B. Kaminska, and J. Rzeszut, "A New Built-In Self-Test Approach for Digital-to-Analog and Analog-to-Digital Converters," Proc. of the *IEEE ICCAD*, 1994, pp. 491-494.

[3] Toner, M.F., and G.W. Roberts, "A BIST Scheme for an SNR Test of a Sigma-Delta ADC," Proc. of the *IEEE ITC*, 1993, pp. 805-814.

[4] Milor, L., *et al.*, "Optimal Test Set Design for Analog Circuits," *IEEE ICCAD*, 1990, pp. 294-297.

[5] Wagner, K.D., and T.W. Wiliams, "Design for Testability of Mixed-Signal Integrated Circuits," Proc. of the *IEEE ITC*, 1988, pp. 823-829.

[6] Soma, M., "A Design-for-Test Methodology for Active Analog Filters," Proc. of the *IEEE ITC*. 1990, pp. 183-192.

[7] Fasang, P.P., D. Mulins and T. Wong, "Design for Testability for Mixed Analog/Digital ASICS," Proc. of the *IEEE CICC*, 1988, pp. 16.5.1-16.5.4.

[8] Max, S., "Fast, Accurate and Complete ADC Testing," Proc. of the *IEEE ITC*, 1989, pp. 598-640.

[9] Souders, T.M., and D.R. Flach, "An Automated Test Set for High Resolution Analog-to-Digital and Digital-to-Analog Converters," *IEEE Trans. on Instrumentation and Measurement*, Vol. IM-28, No. 4, Dec. 1979, pp. 239-244.

[10] Teraoca, E., *et al.*, "A Built-In Self-Test for ADC and DAC in a Single-Chip Speech CODEC," Proc. of the *IEEE ITC*, 1993, pp. 791-796.

[11] Bobba, R., *et al.*, "Fast Embedded A/D Converter Testing Using the Microcontrollers's Resources," Proc. of the *IEEE ITC*, 1990, pp. 598-604.

[12] Browing, C., "Testing A/D converters on Microprocessors," Proc. of the *IEEE ITC*, 1985, pp. 818-824.

[13] Naylor, J.R., "Testing Digital/Analog and Analog/Digital Converters," *IEEE Trans. on Circuits and Systems*, Vol. CAS-25, No. 7. Jul. 1978, pp. 526-538.

[14] DePlassche, R.V., "Integrated Analog-to-Digital and Digital-to-Analog Converters," *Kluwer Academic Publishers*, 1994, pp. 240-262.

[15] Song, M., Y. Lee, and W. Kim, "A Clock Feedthrough Reduction Circuit for Switched-Current Systems," *IEEE Journal of Solid-State Circuits*, Vol. 28, No. 2, Feb. 1993, pp. 133-137.

[16] Heriques, B.G., and J.E. Franca, "High-Speed D/A Conversion with Linear Phase Sinx/x Compensation," Proc. of the *ISCAS*, 1993, Vol. 2, pp. 1204-1207.

[17] Lakshmikumar, K.R., R.A. Hadaway, et al., "A High Speed 8-Bit Current Steering CMOS DAC," Proc. of the *CICC*, 1985, pp. 156-159.

[18] Miki, T., Y. Nakamura, *et al.*, "An 80-MHz 8-bit CMOS D/A Converter," *IEEE Journal of Solid State Circuits*, Vol. SC-21, 1986, pp. 983-988.

[19] Schouwenaars, H.J., *et al.*, "A Monolithic dual 16-Bit D/A Converter," *IEEE Journal of Solid-State Circuits*, Vol. SC-21, No. 3, June 1986, pp. 424-429.

[20] Schouwenaars, H.J., *et al.*, "A Low Power Stereo 16-bit CMOS D/A Converter for Digital Audio," *IEEE Journal of Solid-State Circuits*, Vol. 23, No. 6, Dec. 1988, pp. 1290-1297.

3.3 "Efficient and Accurate Testing of Analog-to-Digital Converters Using Oscillation Test Method"

L'approche de BIST présentée dans la section précédente peut seulement être appliquée aux convertisseurs analogiques/numériques ayant un convertisseur numérique/analogique dans leur structure interne. Pour remédier à ce problème, nous présentons dans cette section une technique de test qui est applicable à n'importe quel type de convertisseurs analogiques/numériques.

Récemment, une nouvelle méthode de test basé sur la transformation du circuit sous test à un oscillateur a été présentée dans la littérature [9]. Après la transformation du circuit, la fréquence d'oscillation est utilisée comme une mesure de test pour juger si le circuit sous test est défectueux ou non. Cette méthode appelée le test par oscillation est très prometteuse pour l'implantation efficace et pratique des structures de BIST car elle n'a pas besoin d'un générateur des vecteurs de test. De plus, la sortie de test est un signal numérique qui peut être analysé dans la puce avec des circuits purement numériques.

Les avantages de la méthode de test par oscillation par rapport aux autres méthodes de test nous ont convaincu de l'adopter pour le test des convertisseurs de données. Dans cette section, des approches de BIST pour la vérification des convertisseurs analogiques/numériques basées sur la technique de test par oscillation seront présentées.

Le travail présenté dans cette section a été soumis pour publication dans *IEEE Transactions on Instrumentation and Measurement.*

Efficient and Accurate Testing of Analog-to-Digital Converters Using Oscillation-Test Method

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Abstract

This paper describes an automatic test approach for analog-to-digital converters (ADCs) based on the oscillation-test strategy. The oscillation-test is applied to convert the ADC under test to an oscillator. The oscillation frequencies are able to monitor the ADC conversion rate, equivalent RMS input noise, differential nonlinearity (DNL) and integral nonlinearity (INL) at each quantization band edge (QBE). These are considered to be the most important characteristics of ADCs. Using this method, no analog stimulus needs to be supplied and therefore the need for a costly precision signal generator is eliminated. Besides, as the oscillation frequency is evaluated using pure digital circuitry, test accuracy is increased. Practical experimentation using real-world successive approximation and flash ADCs confirms the accuracy of the proposed test approach for functional testing of ADCs. Simulation results using a 3-bit flash ADC are also presented. The oscillation-test

has also been applied to the structural testing of dual-slope and sigma-delta ADCs. Both hard and soft faults are considered and some simulation results are presented.

1 Introduction

Analog-to-digital converters (ADCs) are the most frequently encountered mixed-signal circuits. In many industrial and medical applications, ADCs include the sole analog part of the system. Since effective methods for testing the digital part are known, developing practical test approaches for ADCs is clearly important. ADCs are precision products and their test requires reference circuits with at least two more bits of resolution than the circuit under test (CUT). Implementation of these reference circuits results in significant area overhead, which calls into question the practicality and reliability of on-chip methods for ADC testing. Many methods for the on-chip testing of ADCs have been presented in the literature. The digital-to-analog converter (DAC) testing approach has been mapped to test ADCs which use a DAC in their architecture [1],[2]. The built-in self-test (BIST) approach presented in [3] requires that both DAC and ADC be available on the same chip and uses an off-chip DAC and external logic testing equipment. Conventional test techniques have been applied to embedded ADCs using microcontroller resources available on the same chip [4]-[6]. A digital BIST for a signal-to-noise-ratio test of an over-sampled ADC, based on an available DSP core, has also been presented [7]. Each of the above-mentioned BIST approaches is applicable to either a specific ADC type or a specific application, which for example, guarantees the existence of extensive on-chip computational ability.

Testing analog integrated circuits can be accomplished using functional (and/or parametric) verification, DC testing, power-supply current (I_{DDQ}) monitoring, DSP techniques, and the oscillation-test [8],[9].

The oscillation-test method consists of converting the CUT to a circuit which oscillates. The oscillation frequency, which depends directly on the inherent characteristics of the CUT, is evaluated. The deviation of the oscillation frequency from its nominal value indicates a faulty circuit. This test method does not require the test vector generation and application procedure. Furthermore, the oscillation frequency can be considered as a digital signal and can be easily evaluated using pure digital circuitry, increasing the precision of the test. Considering these advantages, the oscillation-test seems to be an effective and practical method for testing ADCs. This paper will describe a new test approach, based on the oscillation-test strategy, for all types of ADCs. This test technique is suitable for both on-chip and off-chip testing situations.

The paper is organized as follows: Section 2 describes ADC error definitions. The proposed test structure for functional testing of ADCs is introduced in section 3. Section 4 presents ADC conversion-time, DNL, INL, and equivalent RMS input noise testing procedures. An alternative test approach for structural testing of ADCs is introduced in section 5. Section 6 describes an alternative approach to testing over-sampled sigma-delta ADCs.

2 ADC Error Definition

In an ADC, a digital number at its output represents a certain input signal interval. In order to precisely measure the errors in an ADC, the input vectors close to a quantization

band edge (QBE) voltage must be used. In other words, the threshold between adjacent quantization intervals, which occurs at a certain voltage, must be determined.

Fig. 1 depicts the probability of the codes C_i and C_{i+1}, corresponding to the quantization intervals Q_i and Q_{i+1} below and above a threshold level V_{Ti+1}, for an ideal and a real ADC in a simplified fashion. Threshold voltage V_{Ti+1} is defined as the point where C_i and C_{i+1} exhibit the same probability of 0.5. In Fig. 1, $V^A_{Ti+1}(V^N_{Ti+1})$ represents the actual (nominal) value of the threshold voltage between codes i and $i+1$, $Q^A_i(Q^N)$ and $Q^A_{i+1}(Q^N)$ are the actual (nominal) quantization intervals below and above a threshold voltage $V^A_{Ti+1}(V^N_{Ti+1})$. As shown for a real ADC in Fig. 1, the V^A_{Ti+1} is displaced from its nominal value, V^N_{Ti+1}, due to the existence of error in a real ADC.

To obtain the ideal characteristics of an ADC, the nominal values of the threshold voltage and quantization band must be found for each input code yielding the theoretical staircase shape as a reference.

Deviation of the threshold levels from their theoretical values causes different sizes of quantization intervals, and this is called differential nonlinearity (DNL). The accumulation effect of DNL errors changes the slope of the staircase over the full range, which is characterized by gain error (G_{FSE}) and integral nonlinearity (INL) error. DNL is defined in terms of the ideal least-significant-bit (LSB) value of the data converter

$$\varepsilon_{i,i-1} = \frac{Q^A_i - Q^N}{Q^N} \tag{1}$$

in which Q^N is equal to 1 LSB. INL error can be calculated by accumulating the various different DNLs

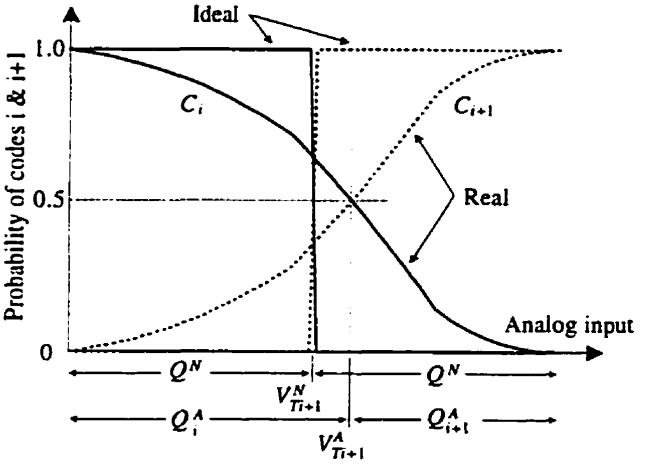


Fig. 1: QBE behavior of ideal and real ADCs. Nominal values are related to ideal ADCs and actual values are related to real ADCs.

$$\varepsilon_i = \sum_{j=1}^{i} \varepsilon_{i,i-1} \tag{2}$$

INL error at the transition level can be measured directly using the following relationship:

$$\varepsilon_i = V_{Ti}^A - V_{Ti}^N \tag{3}$$

where

$$V_{Ti}^N = (i - \tfrac{1}{2})\text{LSB} \tag{4}$$

Conversion-time is also an important parameter for data converters, especially in applications where high-speed operations are need to be performed. It is defined as the time required for an ADC to perform a complete conversion. It should be noted that conversion-time is not necessarily the inverse of the maximum word rate of an ADC, for example in pipeline ADCs.

The best parameter for characterizing the noise behavior of ADCs is its equivalent RMS input noise E_{ni}, that is, the RMS value of the effective internal noise of an ADC, referred to its input terminals. E_{ni} is independent of ADC quantization noise which is due to its nonlinearity property.

3 Proposed Test Structure

The heart of the test , structure for ADCs is a feedback loop which forces the ADC under test to oscillate around a predetermined code or codes. The oscillation frequencies of the two least significant bits of the ADC under test correspond to important parameters of the ADC, such as conversion-time, equivalent RMS noise and DNL, as will be explained later in this paper. Fig. 2 illustrates the block diagram of the test structure which is based on a feedback approach. This test structure considers the ADC under test as a black box, and therefore can be applied to any type of ADC. The device must be operated in the free-running mode by establishing a proper connection between the *End of conversion* output and *Start conversion* input. In other words, the ADC is assumed to be contiguously converting its input voltage. However, to ensure start-up under all possible conditions, a *Start conversion* pulse is required at the beginning of the test procedure. Fig. 3 illustrates the oscillation of the ADC under test around two predetermined codes, C_j and C_k ($C_k > C_j$). All operations are directed by a control logic (CL) which continuously verifies the actual output code C_x of the ADC. If $C_x = C_j$, the input of the integrator is switched to a current I_2 and the input voltage of the ADC under test V_{IN} increases until the control logic detects $C_x = C_k$, whereupon the switch is changed to position I_1 ramping down the ADC input voltage. The switch S passes the current I_1 until the ADC reproduces code C_j, and the procedure is repeated. Neglecting the operation delay of the control logic, the period of oscillation is given by

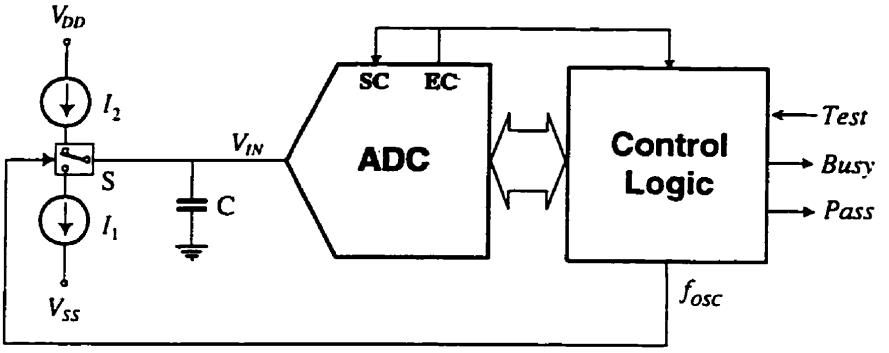


Fig. 2: ADC test configuration (*SC*: Start conversion, *EC*: End of conversion).

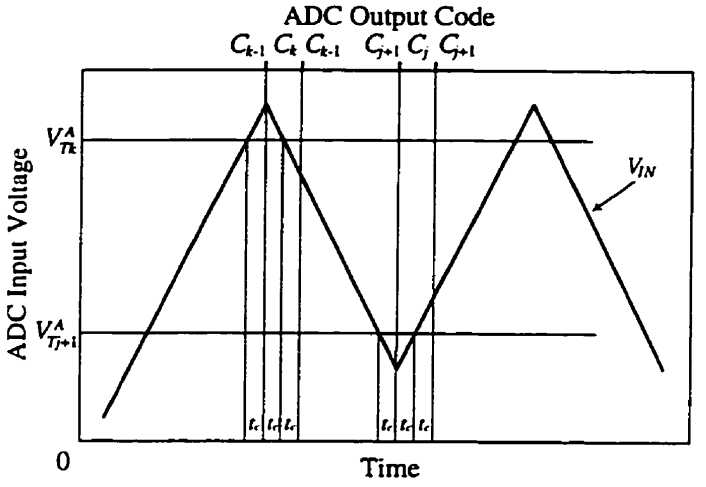


Fig. 3: ADC input voltage oscillation between V_{Tk} and V_{Tj+1} transition thresholds.

$$T = \frac{(V^A_{Tk} - V^A_{Tj+1})C}{I_2} + \frac{(V^A_{Tk} - V^A_{Tj+1})C}{I_1} + 4t_C \tag{5}$$

where t_C is the conversion-time of the ADC under test and C represents the capacitor shown in Fig. 2. Considering $I = I_1 = I_2$, the oscillation frequency is

$$f_{osc} = 1\Big/\left(\frac{2(V^A_{Tk} - V^A_{Tj+1})C}{I} + 4t_C\right) \tag{6}$$

It is necessary to note that in the special condition $k = j+1$, the proposed test structure approaches a classic test technique called the servo-loop method [10]. The servo-loop method, which is well known for its high degree of accuracy, is used to detect the ADC transition voltages. The main difference between the servo-loop method and our test technique in this special condition is the following. In the servo-loop technique, the detected transition voltage is filtered to eliminate the oscillations around the transition voltage and is then compared with a reference voltage produced by a DAC having at least two more bits of resolution. Sometimes the transition voltage obtained is directly converted to digital, using a much more accurate reference ADC, and the ADCs' output codes are compared for each transition voltage [11].

The conventional servo-loop method therefore requires a filter and an accurate reference DAC or ADC which cannot be provided in BIST solutions. In our test technique, the objective is not to directly measure the transition voltages. In fact, we only evaluate the oscillation frequency and deduct the important functional ADC parameters. Therefore, no reference DAC or ADC is necessary and practical on-chip implementation is possible. Furthermore, our technique is more comprehensive and is used to measure a wide range of ADC characteristics.

3.1 Frequency-to-Number Converter (FNC)

In order to evaluate the oscillation frequency coming from a building block in the test mode or a temperature sensor, it is first converted to a corresponding number. Fig. 4 shows the block diagram of the FNC. It uses a simple and fully digital circuit which converts each frequency to a related number. The oscillation frequency f_{osc} of the selected building block is first passed through a level-crossing detector (LCD) to obtain a

rectangular waveform compatible with logic levels and is then applied to a counter. The counter is enabled by the high level of a reference frequency (f_{REF}), and therefore during the high state of the reference frequency the counter counts, and during its low state the counter is disabled and stops counting. The output value of the counter contains a number which is related to its input frequency, coming from the building block under test, and can be evaluated by the CL during the low-state of f_{REF}. The CL resets the counter after evaluating its output number. Therefore, an accurate frequency-to-number conversion is obtained. The accuracy of the system is determined by the reference frequency and the bit number of the counter M. The digital output value is given by

$$B_{1:M} = \frac{f_{OSC}}{2f_{REF}} \tag{7}$$

This technique provides a very good accuracy and satisfies the requirements of our application.

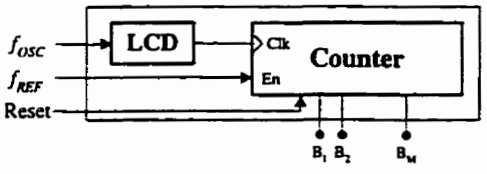


Fig. 4: Block diagram of frequency-to-number converter (LCD: level-crossing detector).

Fig. 5 shows a schematic representation of the LCD implemented in CMOS technology and its transfer curve. The LCD has been designed using a CMOS current-source inverter which acts as a comparator. The current source is a common gate configuration using a p channel transistor with the gate tied to a dc bias voltage. The bias voltage has been adjusted to obtain a trip voltage V_{TRP} of 1 V. The trip voltage is

approximated by the input voltage required to make the current of the transistor M1 equal to the bias current I_B. The gain of the comparator is given as

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m1}}{g_{ds1} + g_{ds2}} = \left(\frac{2K'_N W_1}{L_1 I_B}\right)^{1/2} \left(\frac{-1}{\lambda_1 + \lambda_2}\right) \tag{8}$$

where W_1 and L_1 are the effective channel width and length, $K'_N = \mu C_{OX}$ is the transconductance parameter and λ is the channel length modulation parameter of the transistor M1.

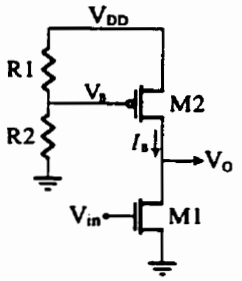


Fig. 5: Schematic representation of the level crossing detector (LCD). The W/L of transistors M1 and M2 are 5μm/1.2μm and 3μm/1.2μm respectively.

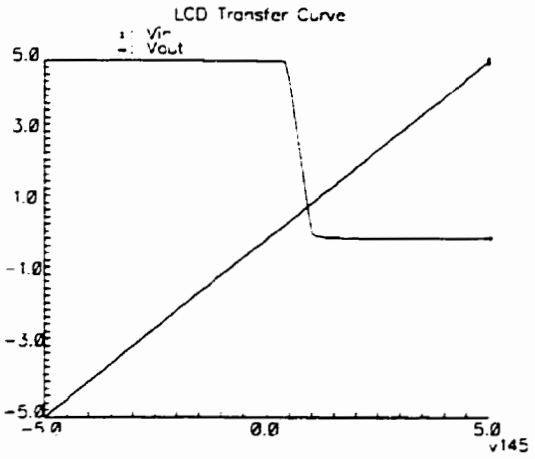
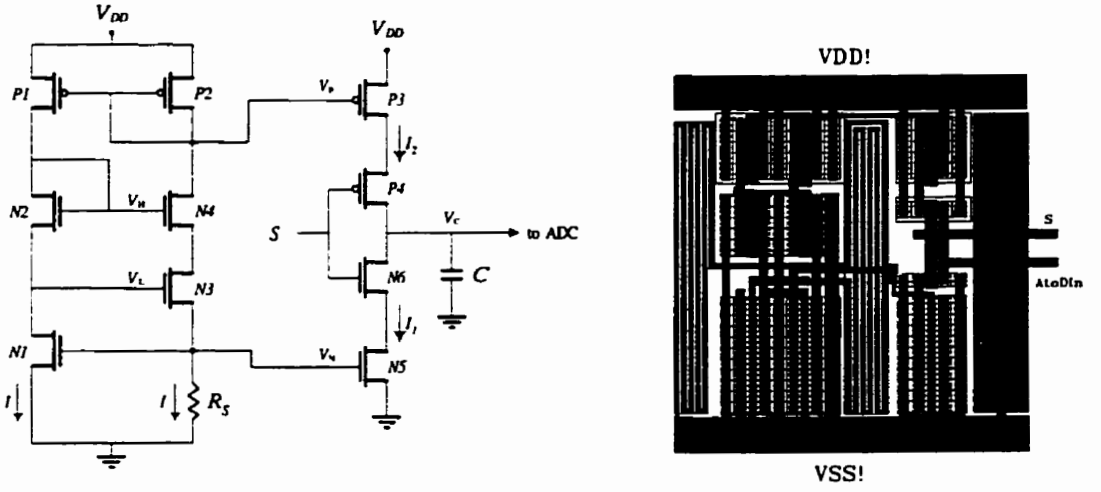


Fig. 6: Transfer curve of the LCD.

An 8-bit resolution FNC comprising the LCD and a synchronous counter has been designed using CMOS 1.2 μm technology and occupies 580 μm^2 of silicon area.

3.2 Reference Current Generation

The noise contributed by current sources is very small in comparison with the noise of the ADC under test and therefore does not affect the measurements. The main error source due to hardware limitations is introduced by the mismatch error between the I_1 and I_2 currents, which causes a difference in the positive and negative rates of the input voltage of the ADC. Reference currents I_1 and I_2 must be designed to match each other as closely as possible. Fig. 7(a) illustrates an implementation of these current sources. The layout of this design using CMOS 1.2 μm technology is presented in Fig. 7(b).



(a) (b)

Fig. 7: Implementation of the analog section of the test circuitry including current sources, switches and the capacitor (a) and its corresponding layout using CMOS 1.2 μm technology (b).

A supply-voltage independent reference current of I_{REF} is set up using transistors N1-N4, P1, P2 and resistor R_S. This current is mirrored in transistors N5 and P3 to produce I_1 (sink) and I_2 (source) respectively. In either case, the current mirrors copy the same reference current, thus ensuring good source/sink current matching. The absolute value of the reference current I_{REF} can be changed to control the currents I_1 and I_2.

4 ADC Testing

In this section, the details of measuring different characteristics of the ADC under test by observing an oscillation frequency are given. A real 8-bit successive approximation and flash ADCs have been used to validate the proposed test methodology. A 3-bit full flash ADC, as shown in Fig. 8, has been designed using a CMOS 1.2 μm technology to investigate the fault detection ability and verify the various different test phases proposed.

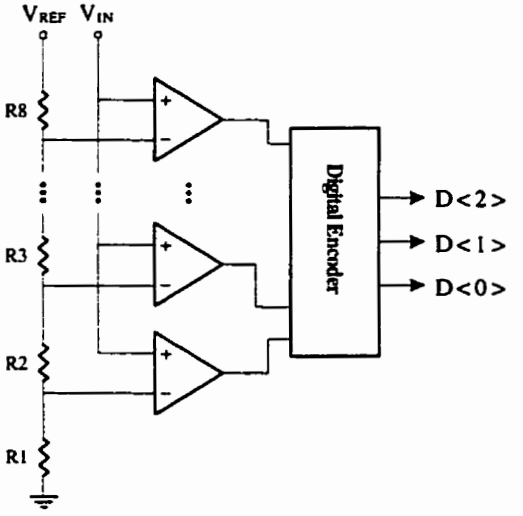


Fig. 8: Circuit diagram of a 3-bit flash ADC (R2 = R3 = R4 = R5 = R6 = R7 and R1 = R8 = R2/2).

4.1 Conversion-time Testing

The test set-up shown in Fig. 2 can be used for determining the conversion-time t_C of the ADC under test for each possible output code. As illustrated in Fig. 9, to measure the conversion-time of a given output code, i.e. C_k, the ADC input is locked to V_{Tk}^A using the feedback loop which forces the ADC output to oscillate between C_k and C_{k-1}. The control logic selects the current I_2, which results in increasing V_{IN}, and compares the output of the ADC with the predetermined code C_k,. When V_{IN} reaches the V_{Tk}^A, after the ADC conversion-time t_C within which the V_{IN} continues increasing, the output code of the ADC will change to C_k, and consequently the current I_1 is selected and the current I_2 is disabled to ramp down the V_{IN}. As I_1 is supposed to be equal to I_2 it also takes t_C for V_{IN} to equal V_{Tk}^A and another t_C to change the output of the ADC to C_{k-1}. By detecting the C_{k-1}, the control logic changes the switch position to select the current I_2 and disable I_1. This process is repeated to oscillate the V_{IN} around V_{Tk}^A, and ADC output code between C_k and C_{k-1}.

From Fig. 9 the f_{OSC} is found to be

$$f_{osc} = \frac{1}{4t_C} \tag{9}$$

which is a special condition of equation (6) where the two different transition voltages are similar. The ADC conversion-time is therefore given by

$$t_C = \frac{1}{4f_{osc}} \tag{10}$$

The oscillation frequency is converted to a digital number and compared with a reference number to evaluate the conversion-time. It is obvious that f_{OSC} does not depend on the capacitor C and current I values, but they must be chosen to keep V_{IN} between

V^A_{Tk-1} and V^A_{Tk+1} or $It_C/C < \text{LSB}$. In other words, the peak to peak amplitude of oscillation V_{IN} must be smaller than 2 LSB. As explained later in this paper, the inferior amplitude limit of V_{IN} is determined by the equivalent RMS input noise of the ADC under test. Measuring the conversion-time at major transition codes is normally sufficient for testing this dynamic parameter.

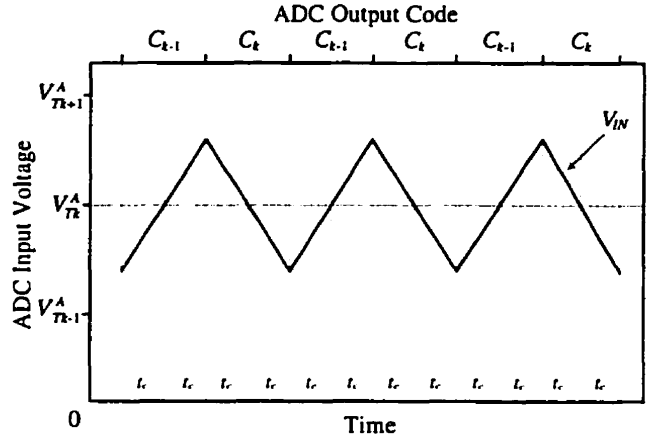


Fig. 9: ADC input voltage oscillation in the vicinity of V_{Tk} to measure the ADC conversion-time t_C.

We have measured the conversion-time of two real ADCs (successive approximation and flash) in practice. The results (55 μs and 1.6 μs) agree with the values reported on the device data sheets. Fig. 10 shows some of the simulations performed to measure the conversion-time of the designed 3-bit ADC. The ADC's input voltage is oscillating around V_{TK}=1.07 V which is the transition voltage between the code 001 and 010.

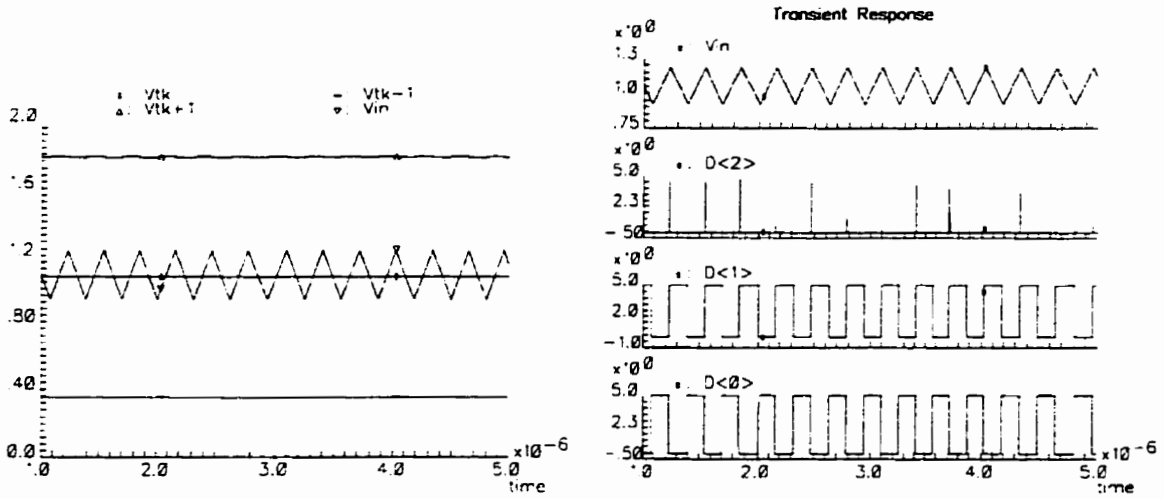


Fig. 10: The oscillation of the 3-bit ADC's input V_{IN} around the transition voltage V_{TK} =1.07 V (a) and its output code between 001 and 010 (b) to test conversion time when the ADC is fault-free.

4.2 DNL Testing

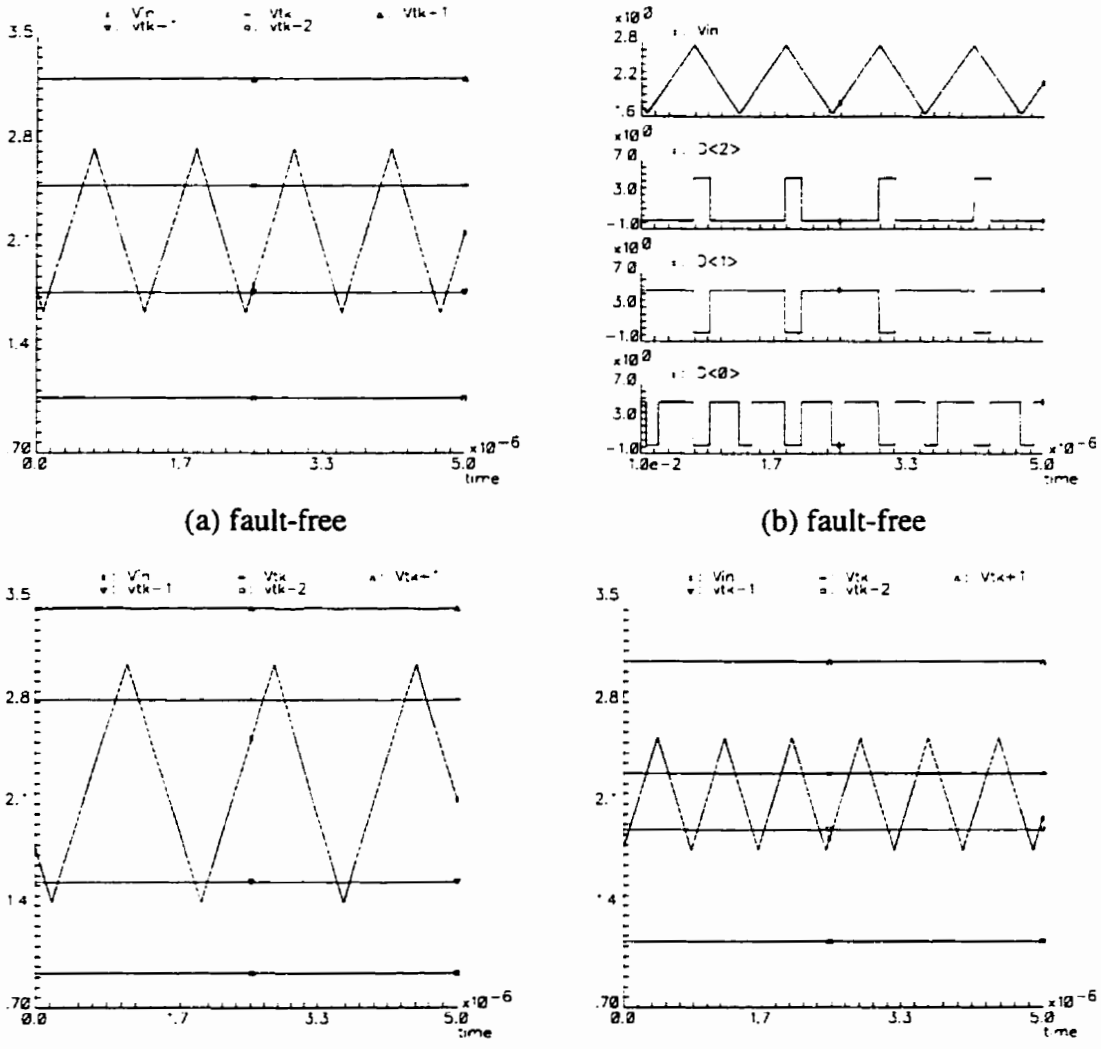
In order to measure DNL at a specified code C_k, using the test configuration in Fig. 2, the ADC output must be forced to oscillate between C_k and C_{k-2}. Consequently, V_{IN} oscillates between V^A_{Tk} and V^A_{Tk-1}. Using equation (6), the oscillation frequency is described by

$$f_{osc} = 1\Big/\left(\frac{2(V^A{}_{Tk} - V^A{}_{Tk-1})C}{I} + 4t_C\right) \tag{11}$$

$$Q^A_k = V^A{}_{Tk} - V^A{}_{Tk-1} = \frac{I}{2C}\left(\frac{1}{f_{osc}} - 4t_C\right) \tag{12}$$

in which the term $4t_C$ has already been measured during conversion-time testing. The oscillation frequency is converted to a number using FNC and is then compared with a predetermined number which represents the nominal value of the oscillation frequency.

This technique has been applied to the real off-the-shelf successive-approximation ADC to obtain an error plot for DNL data. The obtained frequency for each code was subtracted from a reference frequency and divided by the same frequency to obtain the DNL error. Note that the reference frequency represents 1 LSB.



(a) fault-free

(b) fault-free

(c) fault in R_4 (+100%)

(d) fault in R_4 (-50%)

Fig. 11: Testing DNL error of the 3-bit flash ADC under test for V_{Tk-1} = 1.79 V and V_{TK} = 2.51 V. The ADC's output oscillates between 010 and 100.

The 3-bit ADC has also been simulated to measure all possible DNL data. Fig. 11 shows some samples of simulations carried out to test the DNL error of the 3-bit ADC without fault and in the presence of a fault. The ADC's input oscillates between two adjacent threshold voltages V_{Tk-1} = 1.79 V and V_{TK} = 2.51 V. Consequently, the ADC's output code oscillates between 010 and 100 (010 → 011 → 100 → 011 → 010).

4.3 INL and Gain Error Testing

INL error can be calculated by accumulating DNL errors, as defined in equation (2). At a specific code C_k, the control logic measures the DNL error and then adds this DNL error (respecting its sign) to the previous INL error, calculated for C_{k-1}, to obtain the INL error for C_k. The INL error for the most significant code C_k = (11 ... 1) is called gain error. The INL measurement will be corrupted by DNL errors if DNL data are not accurate.

The INL at a given code C_k can also be evaluated directly by forcing the ADC input to oscillate between C_0 (00 ... 0) and C_{k+1}. Consequently, V_{IN} oscillates between V_1^A and V_{Tk+1}^A. Using equation (6), the oscillation frequency is found to be

$$f_{osc} = 1 \Big/ \left(\frac{2(V^A{}_{Tk+1} - V^A{}_1)C}{I} + 4t_C \right) \tag{13}$$

$$\varepsilon_k = (V^A{}_{Tk+1} - V^A{}_1) - (V^N{}_{Tk+1} - V^N{}_1) \tag{14}$$

Using equation (4) $V^N{}_{Tk+1} - V^N{}_1 = k \times \text{LSB}$ and therefore the oscillation frequency represents the actual value of k LSB that is the ideal input voltage of the output code C_k. The INL error can thus be evaluated by comparing this oscillation frequency with its nominal frequency value, which represents k LSB. As INL data can be obtained from

DNL data and vice versa, they can be considered as redundant data. In general, if DNL is tested for all possible output codes, testing INL at some critical point is sufficient to characterize the ADC under test [1].

4.4 Equivalent RMS Input Noise Testing

As ADC resolution approaches its noise level, the probability of bit errors greatly increases. Therefore, evaluating noise is indispensable for medium- to high-resolution ADCs. Three noise measurement techniques have been applied to ADCs.

The first technique consists in digitizing a pure sinewave by the ADC under test and measuring the noise contributed by the ADC [7],[12]. In fact this technique measures the signal-to-noise ratio at the output of ADCs with respect to a specified input stimulus. This technique is suitable for high-speed, low-resolution applications, but presents many limitations. It requires generating a pure sinewave stimulus with accurate and stable amplitude and frequency which are, in general, not easy to produce for high-resolution ADCs at a reasonable cost. Furthermore, ADC errors such as quantization noise and nonlinearity cannot be separated from the inherent fundamental noise.

The second technique requires a high-resolution digital-to-analog converter (DAC), which has a resolution at least 3 bits greater than the ADC under test. The DAC is used to find the ADC transition levels. Then the input voltage is offset by a small predetermined value and the distribution of the probability of output codes is measured. The equivalent RMS noise is deducted from a few such measurements. Now, having overcome many of the limitations of the first technique, it is still limited, this time by the availability of the required DAC.

In the third technique, ADC noise measurements are taken in proximity to the QBEs [11],[13]. A feedback loop is used to locate and lock the transition levels. With a noiseless ADC, the input voltage will ordinarily oscillate around the transition level with a predetermined amplitude V_{IN}. Supposing that V_{IN} is close to the ADC noise level, the existence of the equivalent RMS input noise at the input of the ADC under test, E_{ni}, disturbs the feedback loop. The ADC input voltage will follow a "random walk" around the transition level instead of regular oscillation and therefore the oscillation frequency is affected by the noise. Assuming that the probability distribution of the noise is Gaussian, the statistics of random walk can be calculated in terms of the RMS noise level.

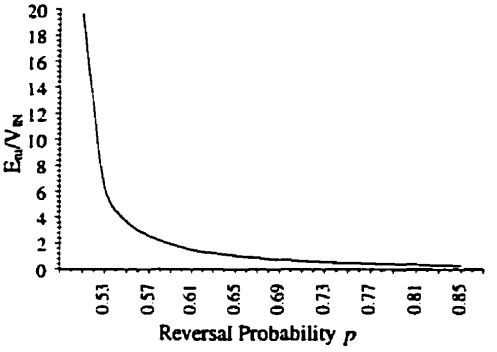


Fig. 12: Relationship between the slope reversal probability p and the noise ratio E_{ni}/V_{IN}..

The probability p of occurrence of a slope reversal at the input of the ADC can be expressed in terms of the ratio E_{ni}/V_{IN}, as shown in Fig. 12 [13]. This relationship has been proven using various experimental results. The reversal probability can be easily measured using digital techniques, and, therefore, knowing the V_{IN} amplitude, the equivalent input RMS noise level can be determined.

This technique seems to be the most promising technique for on-chip measurement of ADC noise level. The proposed test architecture requires a very low-noise wide-band operational amplifier. Also, the offset voltage of the opamp must be very small.

In this paper, we adapt the third noise measurement technique to our test structure to complete the ADC test procedure. It is especially interesting because the required feedback loop may be the same feedback loop employed to measure the ADC conversion-time, DNL error and other static parameters. In our proposed test structure, no operational amplifier is required and therefore the drawback mentioned above is overcome. We employ a new approach to measure the reversal probability p.

The data describing the relationship between p and E_{ni}/V_{IN}, as shown in Fig. 12, has been fitted in a rational function, as follows [14]:

$$E_{ni}/V_{IN} = \frac{-0.7 + 0.6p}{1 - 2p} \tag{15}$$

In order to verify this relationship, we modeled the proposed test structure with a 10-bit ADC using Matlab in a SIMULINK environment. A white noise source has been used to represent the equivalent input noise of the ADC under test. By changing the noise level the E_{ni}/V_{IN} ratio was varied and the reversal probability p was observed. The simulation results agree within 5 percent with previously reported data.

Unlike the previous tests for conversion-time, DNL and INL testing in which the V_{IN} amplitude must be much bigger than the noise level to minimize the effect of noise on the measurements, in this case the V_{IN} amplitude must be adjusted to be comparable with E_{ni} by controlling the I_{REF} value.

The reversal probability is measured by converting the oscillation frequency to a number using the FNC. Knowing the amplitude of V_{IN}, the ADC equivalent RMS input

noise E_{ni} can be estimated from the measured reversal probability p using the equation (15). For BIST structures, pass/fail information can be provided by determining a signature number corresponding to the maximum acceptable E_{ni}/V_{IN} ratio based on a predetermined V_{IN} amplitude. Thus, if the number obtained from the noise measurement procedure is smaller than the test signature, the test result is a pass.

5 Alternative Test Approach for Dual-Slope and Σ-Δ ADCs

Functional tests which characterize all important parameters of the ADC under test are very time consuming, especially for high-resolution ADCs. For example the number of DNL tests grows exponentially with the ADC resolution. In this section, we introduce an alternative approach which consists of structural testing of ADCs based on the oscillation-test strategy. Dual-slope and oversampled sigma-delta ADCs are considered. A two-stage CMOS operational amplifier (OA) shown in Fig. 13 was used to realize the ADCs under test.

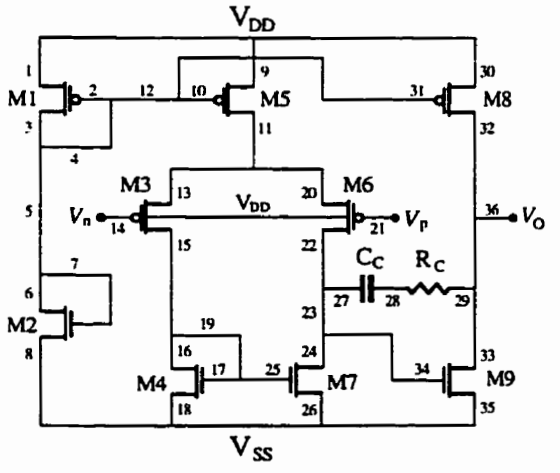


Fig. 13: Compensated CMOS operational amplifier.

To quantify the fault coverage, a comprehensive list of catastrophic faults have been injected in OAs and passive components (R and C). The catastrophic faults considered in this study comprise all open faults at all circuit nodes and short faults between every combination of two nodes at transistor level in opamps, and shorts for all other components. 36 different nodes are identified on OA schematic. Note that some nodes that seem schematically redundant such as 8, 18, 26, and 35 are not physically redundant. The total number of 657 faults, consisting of 27 open faults and 630 short faults ($C_2^{36} = 36!/(2!(36-2)!)$ is used as the fault dictionary for each OA under test. An open fault is simulated by introducing a 10 M ohm resistor and a short fault is modeled by a 10 ohm resistor. Parametric faults in passive components are considered by determining their undetectable limits of variation.

5.1 Dual-Slope ADC Testing

A block diagram of a dual-slope ADC is shown in Fig. 14 in which the dotted lines are used only during the test mode (*TM*). The analog part of the converter comprises an integrator and a comparator. The property of integrating the input signal makes this converter immune to noise. The main advantage of this architecture over the single-slope ADC is that it eliminates the dependency of the conversion process on the linearity and accuracy of the slope. In this structure, it is necessary for V_{IN} to be positive.

At the beginning the integrator is reset and then the input switch selects V_{IN} which is integrated negatively for N_{REF} number of clock cycles. At the end of N_{REF} counts, the input switch selects $-V_{REF}$ and the integrator integrates positively with a constant slope, because $-V_{REF}$ is constant. A counter counts until the comparator input crosses zero which

activates the comparator (OA1) and the counter is stopped. Hence, the actual counter content N_{OUT} numerically represents the analog input V_{IN} as follows.

$$N_{OUT} = N_{REF} \frac{V_{IN}}{V_{REF}} \tag{16}$$

The test procedure is composed of two phases. In the first test phase, the input switch selects the output of the comparator to connect it to the input of the integrator to form an oscillator. Therefore, the oscillator is formed by the integrator and comparator without any additional circuitry. The oscillation frequency is converted to a number by the counter existing in the control logic. The number obtained is compared with a predetermined test signature to verify whether there is a fault in the analog part of the ADC or not.

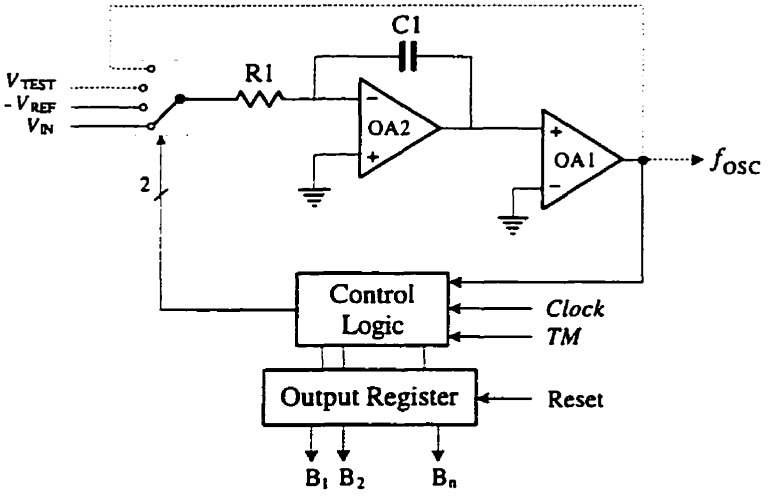


Fig. 14: Block diagram of a testable dual-slope ADC system based on the oscillation-test method (R1 = 50kΩ, C1 = 30 pF).

Note that all analog circuitry of the ADC are involved in the oscillator. In the second test phase, the ADC is rearranged to its functional mode and a voltage reference (V_{TEST}) is converted to its corresponding digital word. The digital number is compared with the second test signature to verify the accuracy of the V_{REF}. All operations are directed by the control logic. In this way, the internal ADC blocks which contribute to the oscillator structure are tested. The simplicity and efficiency of this test architecture are obvious. The area overhead is related to only a small part of the control logic and a feedback loop.

The test time is very short because the test is performed in two phases, equivalent to the time needed to convert two analog signals using the ADC under test. Although this test partially verifies the functionality of the digital part, it is generally assumed that the digital circuitry has been already tested using the BIST method dedicated to the digital part of the chip.

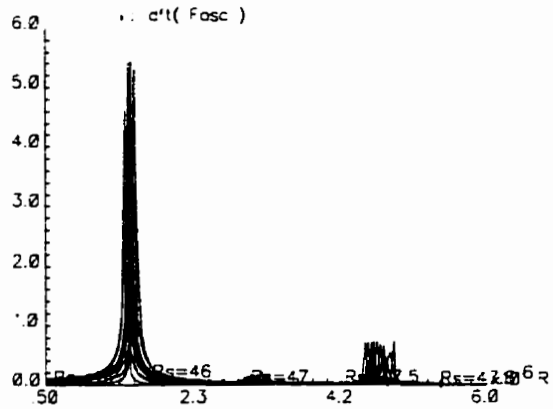
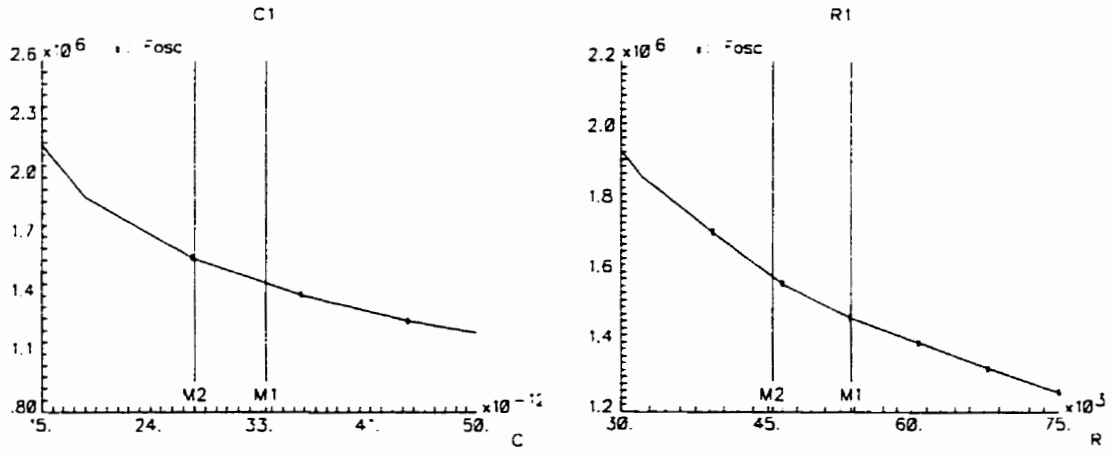


Fig. 15: FFT of the oscillation frequency of the dual-slope ADC in the test mode resulting from Monte Carlo analysis.

A Monte Carlo analysis taking into account all process and design variations has been performed to determine the tolerance band of the oscillation frequency for fault free ADC. To better visualize the tolerance band of the oscillation frequency, the fast Fourier transform (FFT) of the oscillating signal is presented in Fig. 15. The tolerance band is determined to be [-4% , +5.2%].

Faults which deviate the oscillation frequency out of this tolerance band are considered to be detectable. Fig. 16 depicts the undetectable variation limits of passive components of the dual-slop ADC based on the tolerance band of the oscillation frequency determined by the Monte Carlo analysis. The upper and lower limits of the undetectable variation limits of each component are marked by M1 and M2 respectively. The vertical axis represents the oscillation frequency and the horizontal one represents the component value.



a) C1 = 30 pF

b) R1 = 50 kΩ

Fig. 16: The output oscillation frequency of the dual-slope ADC in the test mode versus its passive components. The undetectable limits of parametric faults are marked by M1 and M2.

The result of a comprehensive catastrophic fault simulation for the first test phase is presented in Table 1. The majority of injected faults resulted in loss of oscillation. For the sake of simplicity the faults resulting in the loss of oscillation are not presented in the table. The shadowed faults cannot be detected in this test phase. The fault coverage of the first test phase is about 96.5%.

The second test phase increases the fault coverage to 98%. Fig. 17 illustrates the output signal of the dual-slope ADC in test mode without fault and for some typical injected faults.

Table 1: Comprehensive list of catastrophic faults in OA1 and OA2 (2×657).

Fault	**Output Oscillation Frequency**	**Fault**	**Output Oscillation Frequency**
OA1N6,8-S*	$f_O \approx 1.11\, f_{osc}$	OA1N28-O*	$f_O \approx 2.74\, f_{osc}$
OA1N10,11-S*	$f_O \approx 0.92\, f_{osc}$	OA2N1-O	$f_O \approx 0.96\, f_{osc}$
OA1N31,32-S*	$f_O \approx 0.90\, f_{osc}$	OA2N3-O	$f_O \approx 0.97\, f_{osc}$
OA1N5,15-S*	$f_O \approx 1.28\, f_{osc}$	OA2N6,8-S*	$f_O \approx 0.97\, f_{osc}$
OA1N28,29-S*	$f_O \approx 0.98\, f_{osc}$	OA2N9,11-S*	$f_O \approx 0.85\, f_{osc}$
OA1N1-O	$f_O \approx 1.07\, f_{osc}$	OA2N10,11-S*	$f_O \approx 0.97\, f_{osc}$
OA1N3-O	$f_O \approx 1.06\, f_{osc}$	OA2N28,29-S*	$f_O \approx 1.02\, f_{osc}$
OA1N16-O	$f_O \approx 0.35\, f_{osc}$	OA2N28-O*	$f_O \approx 1.14\, f_{osc}$
OA1N18-O	$f_O \approx 0.46\, f_{osc}$	**1268 *other hard faults***	***No oscillation***

OA1N16-O: Open at the node 16 of the OA1, OA1N6,8-S: Short between nodes 6 and 8 of the OA1, *: Representing a set of schematically redundant faults.

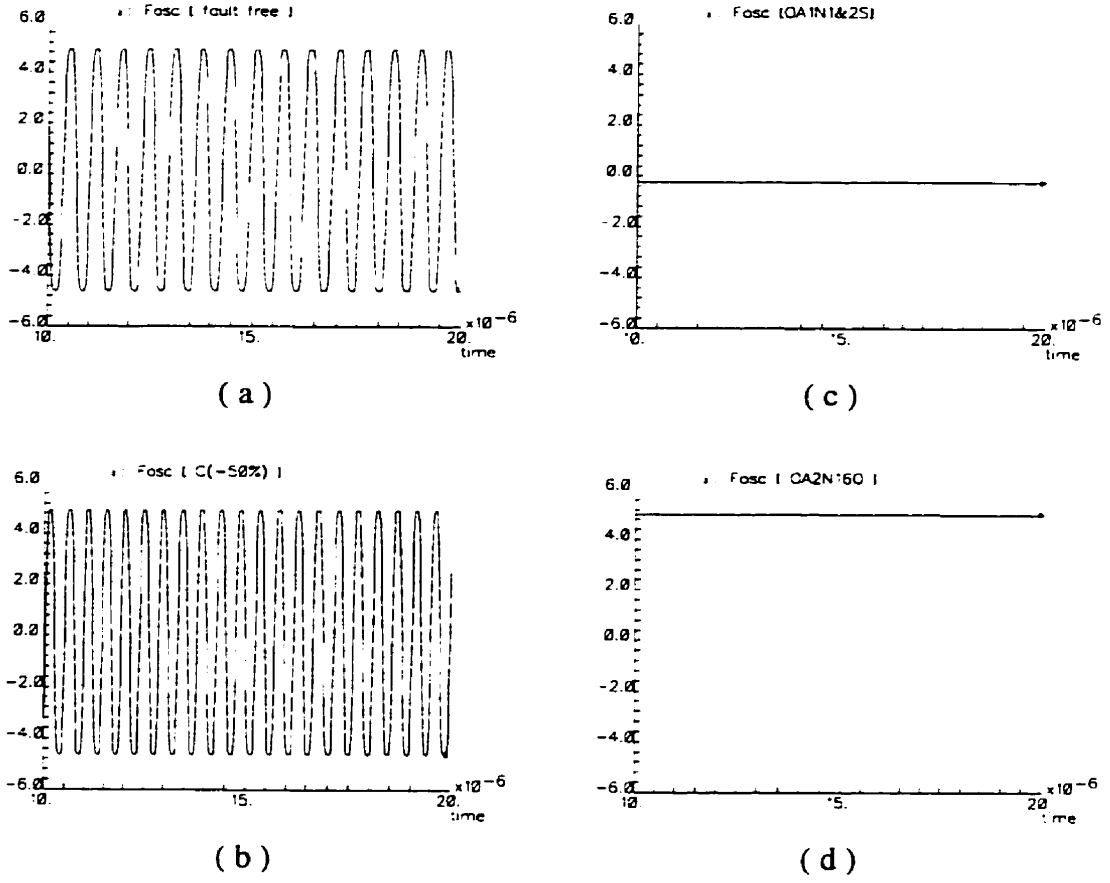


Fig. 17: Dual-slope ADC's output signal in the test mode without fault and in the presence of some typical injected faults (OA1N1&2S: short circuit between nodes 1 and 2 of OA1, OA2N16O: open circuit at node 16 of OA2). The oscillation frequency of the fault-free ADC is 1.53 MHz. Fault in the capacitor C1[-50%] deviates the oscillation frequency to 2.15 Mhz.

5.2 Σ-Δ Modulator Testing

The most widely used oversampled converter consists of a noise shaping converter with a one-bit internal quantizer, called sigma-delta modulator. A complete sigma-delta ADC consists of a sigma-delta modulator and a decimation filter. The analog input is converted

into a series of single-bit digital words at a frequency of much higher than the Nyquist rate using the sigma-delta modulator.

Fig. 18 illustrates a block diagram of a first-order sigma-delta modulator. It is composed of a summing node, an integrator, a 1 bit ADC and a 1 bit DAC in the feedback loop. The integrator makes the loop gain infinite at DC and therefore the DC component of the average of the error signal is zero. When the input is a DC signal, the output quantized signal oscillates between two levels. It can be shown that the sigma-delta modulator has a low-pass effect on the signal and a high-pass effect on the quantization noise which is known as noise shaping property. Therefore, the quantization noise in the signal band is attenuated and noise in the higher frequency region is accentuated.

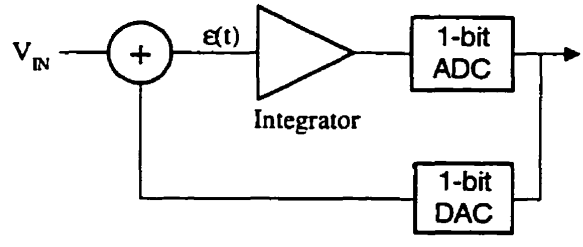


Fig. 18: First-order Σ-Δ modulator.

Fig. 19 shows a testable first-order sigma-delta modulator. Only the dotted lines are added for test purposes. In the functional mode, the *TM* signal puts the switches in the position shown Fig. 19 in which switch *S1* selects the flip-flop output and switch *S2* selects the input voltage V_{IN}. During the test mode, *S1* selects the output of OA1 and *S2* selects either V_{TSET} or ground. In the first test phase, the ADC input voltage V_{IN} is connected to the ground and the circuit oscillates at a predetermined frequency. In the second test phase the input V_{TEST} is applied and the output oscillation frequency is

analyzed. These two oscillation frequencies are converted to a digital code and used as test signatures to monitor faults. The test is completed by a functional test in which the reference voltage V_{TEST} is converted to a digital word using the sigma-delta ADC and the output code is considered as the third test signature.

These three test signatures are used to distinguish between faulty and fault-free sigma-delta converters. It is assumed that the digital part of the ADC is already tested using the BIST structure dedicated to the digital part of the chip. Fig. 20 illustrates the sigma-delta modulator's output signal in the first phase of the test mode without and in the presence of a -20% deviation fault in C1.

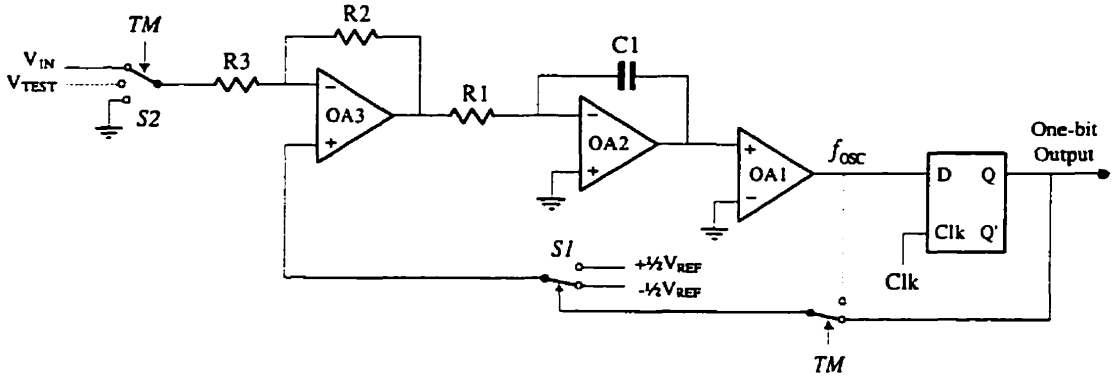


Fig. 19: Schematic of a testable first-order Σ-Δ modulator based on the oscillation-test method (C1=30 pF, R1= 100 kΩ, R2= 10 kΩ, R3= 10 kΩ).

A comprehensive fault simulation analysis showed that a catastrophic fault coverage of around 98.5 % can be achieved. A Monte Carlo analysis taking into account the nominal tolerance of all CUT's components has been performed to determine the tolerance band of the oscillation frequency. The result of Monte Carlo analysis of the sigma-delta

modulator in test mode is shown in Fig. 21. The oscillation frequency tolerance band has been usede to find the undetectable variations of passive components.

Finally, Fig. 22 depicts the undetectable variation limits of some of the sigma-delta modulator elements based on the tolerance band of the oscillation frequency determined by the Monte Carlo analysis. The upper and lower undetectable variation limits of each component are marked by M1 and M2 respectively. The vertical axis represents the oscillation frequency and the horizontal one represents the component value.

In Fig. 22 the variation of oscillation frequency versus component variation for all passive components, the OA1's transistor M6 length OA1LM6, and the OA2's M3 transistor width OA2WM3 is presented. These results demonstrate the capability of the proposed test approach in detecting parametric faults.

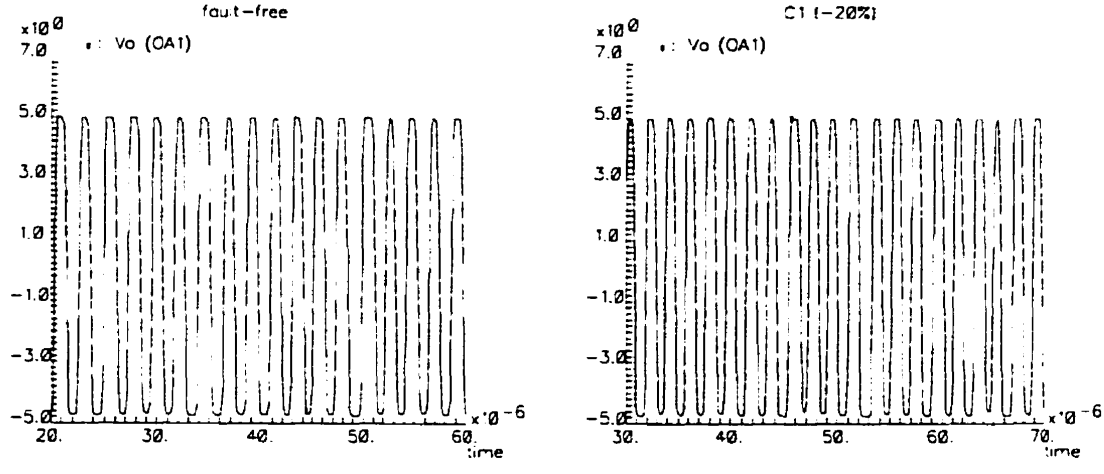


Fig. 20: Sigma-delta modulator's output signal in the test mode without fault and in the presence of a parametric fault in the capacitor C1.

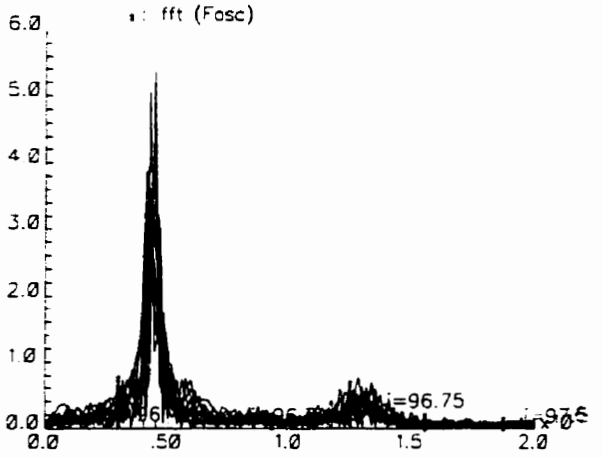
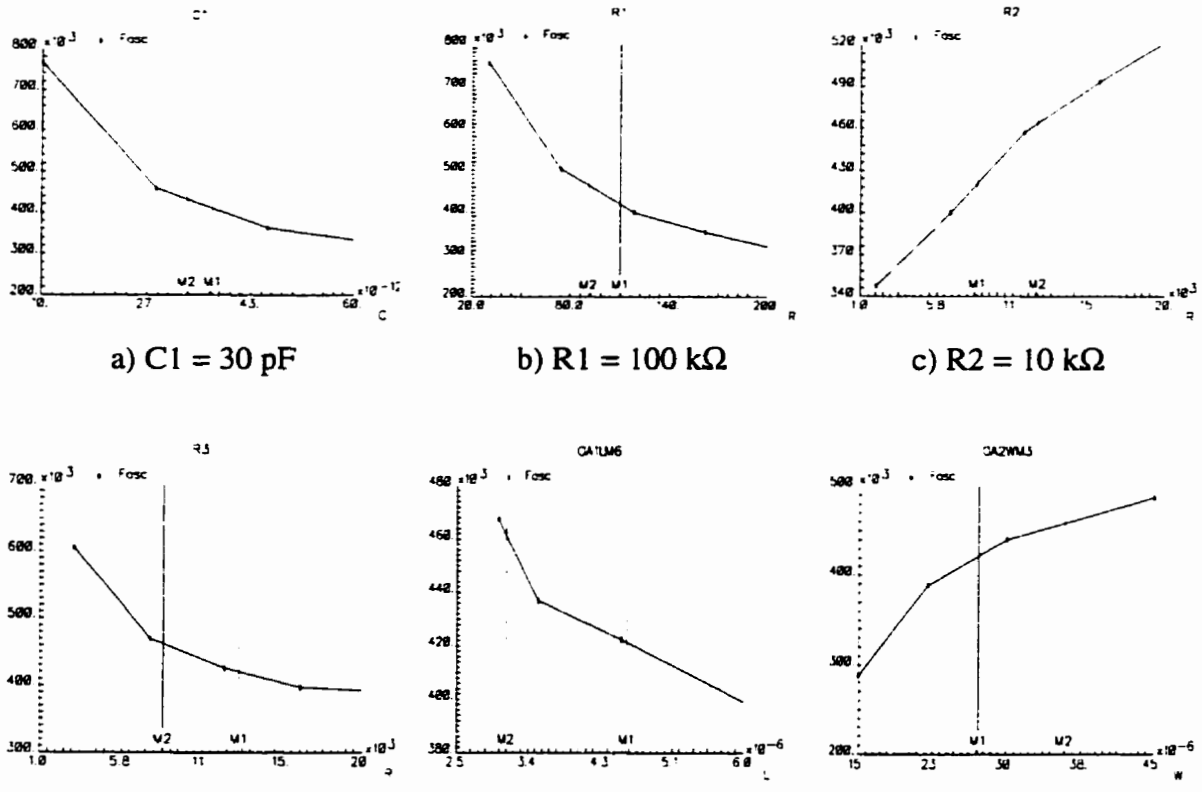


Fig. 21: Fast Fourier transform of the Monte Carlo analysis of the Σ-Δ modulator-based oscillator to specify the tolerance band of oscillation frequency.

All of the results presented in this section are obtained for the first test phase in which the input of the sigma-delta modulator is connected to ground.

In this paper structural testing of a first-order sigma-delta modulator has been considered. Higher order sigma-delta modulators have similar building blocks and therefore the same technique can be extended to address their testability.



a) C1 = 30 pF b) R1 = 100 kΩ c) R2 = 10 kΩ

d) R3 = 10 kΩ e) L_{M6} = 4 μm f) W_{M3} = 30 μm

Fig. 22: The output oscillation frequency of the Σ-Δ modulator in the test mode versus different passive components and transistors width and length (OA1LM6: transistor M6 length of OA1, OA2WM3: transistor M3 width of OA2).

6 Conclusion

A new test technique for complete and accurate testing of ADC has been proposed. This test method is capable of measuring DNL, INL, conversion-time and noise level of the ADC under test without applying a test stimulus. Furthermore, the output of the test technique is an oscillation frequency which can be analyzed using pure digital circuitry, thereby increasing test accuracy. As no voltage or current measurement is necessary, the performance degradation problem and the need for a high precision DAC or ADC are

eliminated. The proposed test technique has been implemented in CMOS 1.2 μm technology of MITEL Semiconductor as a BIST solution for functional testing of an 8-bit flash ADC and the area overhead is only 2 % of the chip active area. The area overhead is related to a small control logic and very simple analog circuitry. As a digital-output test method, it can be easily integrated with the test methods dedicated to the digital part of the chip under test. The validity of the proposed test technique has been verified through extensive simulations using a 3-bit flash ADC and practical discrete realization. The oscillation-test has also been applied to structural testing of ADCs to speed up the test process for the applications where the test-time budget is limited. It can be mentioned that for the examples treated in this paper structural testing resulted in a reduced test time and area overhead, while functional testing provides a high degree of confidence because the CUT specifications are directly tested.

References

[1] Arabi, K., B. Kaminska, and J. Rzeszut, "BIST for Digital-to-Analog and Analog-to-Digital Converters," *IEEE Design & Test of Computers*, Winter 1996, Vol. 13, No. 4, pp. 40-49.

[2] Arabi, K., B. Kaminska and J. Rzeszut, "A Built-In Self-Test Approach for Medium to High Resolution Digital-to-Analog," Proc. of the *IEEE ATS*, 1994, Nara, Japan, pp. 373-378.

[3] Teraoca, E. *et al.*, "A Built-In Self-Test for ADC and DAC in a Single-Chip Speech CODEC," Proc. of the *IEEE ITC*, 1993, pp. 791-796.

[4] Max, S., "Fast Accurate and Complete ADC Testing," Proc. of the *IEEE ITC*, 1989, pp. 111-118.

[5] Bobba R. *et al.*, "Fast Embedded A/D Converter Testing Using the Microcontrollers' Resources," Proc. of the *IEEE ITC*, 1990, pp. 598-604.

[6] Browing, C., "Testing A/D converters on Microprocessors," Proc. of the *IEEE ITC*, 1985, pp. 818-824.

[7] Toner, M.F. and G.W. Roberts, "A BIST Scheme for an SNR Test of a Sigma-Delta ADC," Proc. of the *IEEE Int. Test Conf.*, 1993, pp. 805-814.

[8] Arabi, K. and B. Kaminska, "Parametric and Catastrophic Fault Coverage of Analog Circuits Using Oscillation-Test Methodology," Proc. of the *IEEE VLSI Test Symp.*, Monterey, April 1997, pp. 166-171.

[9] Arabi, K. and B. Kaminska, "Oscillation-Test Strategy for Analog and Mixed-Signal Integrated Circuits," Proc. of the *IEEE VTS*, 1996, pp. 476-482.

[10] Corcoran, J.J., T. Hornak and P.B. Skov, "A High-Resolution Error Plotter for Analog-to-Digital Converters," *IEEE Trans. on Instrumentation & Measurement*, vol. 24, 1975, pp. 370-374.

[11] Souders, T.M. and D.R. Flach, "An Automated Test Set for High-Resolution Analog-to-Digital and Digital-to-Analog Converters," *IEEE Trans. on Instrumentation and Measurement*, vol. 28, 1979, pp. 239-244.

[12] Kerster, W.A., "Characterizing and Testing A/D and D/A Converters for Color Video Applications," *IEEE Trans. on Circuits & Systems*, vol. 25, 1978, pp. 539-550.

[13] Souders, T.M. and D.R. Flach, "An NBS Calibration Service for A/D and D/A Converters," Proc. of the *IEEE ITC*, 1981, pp. 290-300.

[14] Souders, T.M. and J.A. Lechner, "A Technique for Measuring the Equivalent RMS Input Noise of A/D Converters," *IEEE Trans. on Instrumentation and Measurement*, vol. 29, 1980, pp. 251-256.

3.4 "Design for Testability of Embedded Integrated Operational Amplifiers"

Dans les sections précédentes, le problème de test des convertisseurs de données a été abordé. Les convertisseurs de données sont des composants nonlinéaires et en général très précis. Ils sont alors considérés comme des circuits très difficiles à tester. D'autres blocs analogiques utilisés dans les systèmes biomédicaux comme les filtres et les amplificateurs sont considérés dans la catégorie des composants linéaires. Les composants linéaires peuvent facilement être modélisés par une fonction de transfert. Alors, la même approche de test peut être appliquée à la plupart des circuits linéaires.

Comme exemple typique, nous allons traiter le problème de test des amplificateurs opérationnels dans cette section. Avec des modifications simples, la même technique peut être appliquée aux autres circuits linéaires. Comme choix de méthode de test, nous utilisons la technique de test par oscillation introduite tout récemment à cause de sa simplicité et l'efficacité qu'il nous offre pour l'implantation des structures de BIST.

Les résultats de recherche présentés dans cette section ont été acceptés pour publication dans *IEEE Journal of Solid-State Circuits.*

Design for Testability of Embedded Integrated Operational Amplifiers

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Abstract

The operational amplifier (op-amp) is one of the most encountered analog building blocks. In this paper the problem of testing integrated op-amp is treated. A new low-cost vector-less test solution, known as oscillation-test, is investigated to test the op-amp. During the test mode, the op-amps are converted to a circuit that oscillates. The oscillation frequency is evaluated to monitor faults. The tolerance band of the oscillation frequency is determined using a Monte Carlo analysis taking into account the nominal tolerance of all important technology and design parameters. Faults in the op-amps under test which cause the oscillation frequency to exit the tolerance band can therefore be detected. Some design for testability (DFT) rules to rearrange op-amps to form oscillators are presented and the related practical problems and limitations are discussed. The oscillation frequency can be easily and precisely evaluated using pure digital circuitry. Besides, due to its digital nature, it can be interfaced to boundary scan. The simulation and practical implementation

results confirm that the presented techniques ensure a high fault coverage with a low area overhead.

1 Introduction

Unlike digital circuits, the specifications of analog circuits are usually very varied which render their test and characterization very difficult and time-consuming. During the past ten years, extensive research has been devoted to analog and mixed-signal testing. Testing analog circuits can be accomplished using functional (and/or parametric) testing [1]-[4], DC testing [5],[6], quiescent power-supply current (I_{DDQ}) monitoring [7],[8], and digital signal processing (DSP) techniques. Various design for testability (DFT) rules compatible with the above mentioned test methods have been developed to increase the controllability and observability of the circuit under test. Unfortunately there is not a generally accepted test technique for analog and mixed-signal circuits.

The integrated operational amplifier is the most widely used linear active circuit in today's mixed-signal systems. This active element has very high differential-mode open-loop gain and input impedance. For analog functional blocks with embedded op-amps, the test procedure will be easier and the fault coverage will be higher if we assume that the op-amps are fault-free. Therefore, it is important to have an efficient technique to test integrated op-amps. The problem of testing integrated op-amps has been addressed by many researchers. Op-amp power supply control has been proposed in [9] and [10] as an approach to expose faults. As it requires varying the power supply voltage of the CUT, its integrated implementation causes some problems. I_{DDQ} testing [11] technique has resulted in a fault coverage of less than 90%. Current sensing necessitates at least one transistor to be cascoded with the circuit under test between supply rails which introduces performance degradation. The simplicity of the DC voltage test method was the driving

force behind the evaluation of its effectiveness for op-amps. The percentage of faults detected by DC voltage test using primary inputs and outputs is around 80% excluding the capacitor faults which cannot be detected by DC tests [12]-[14]. To increase the fault coverage, the op-amp internal nodes must also be observed and the test must be completed by some additional dynamic tests [12] or the circuit redundancy must be eliminated during the design stage [13].

Another problem common to the majority of test methods consists of determining an optimal set of excitation signals and test points. Oscillation-test has shown to have the potential of overcoming most of the above mentioned problems [15]-[18]. The effectiveness of this test strategy for op-amps is examined in this paper. The paper is organized as follows. Section 2 introduces a brief description of oscillation-test method. Design and Modeling of operational amplifiers are presented in section 3. Several DFT techniques for op-amps are introduced in Section 4. A technique to measure the gain-bandwidth is proposed in section 5. Section 6 discusses important practical issues.

2 Oscillation Test Methodology's Basic Definitions

A brief description of the oscillation-test method is given in this section. A set of definitions necessary to evaluate the parametric and catastrophic fault coverage of analog circuits is also introduced. These definitions prevent many confusions due the lack of clear and common understanding about basic characteristics of analog testing by unifying the interpretation of each notion.

Oscillation-test method is based on partitioning a complex analog circuit into functional building blocks, such as amplifier, operational amplifier (OA), comparator, Schmitt trigger, filter, voltage reference, oscillator, phase lock loop (PLL), etc., or a

combination of these blocks. CUT partitioning offers the possibility of fault diagnosis at building block level and also make it possible to detect multiple faults providing that they occur in different building blocks. During test mode, each building block is converted to a circuit which oscillates. The oscillation frequency ω_{osc} of each building block can be expressed as a function of either its components or its important parameters. The building blocks which inherently generate a frequency, such as oscillators, do not need to be rearranged, and their output frequency is directly evaluated. The test is performed by evaluating the oscillation frequency. The main supposition is that the oscillation frequency is produced by the CUT components and therefore a fault in these components will affect the oscillation frequency. In the following, some basic definitions which are necessary to understand the test procedure are given. These definitions let evaluate and compare the effectiveness of different test solutions.

Definition 1: Tolerance Limits of a Parameter

Tolerance limits of a parameter P_i are defined to be the maximum acceptable variations of that parameter in the CUT.

Parameters are functional characteristics of an analog circuit such as gain, cut-off frequency, bandwidth, etc. which are fixed by the designer to fulfill the required specifications. In some cases, the tolerable variations of a parameter is only determined by its upper or lower limit. For example the tolerable variation of the central frequency of a band-pass filter is determined by its lower and upper limits, but the tolerable variations of the gain-bandwidth of a operational amplifier is only determined by its lower limit.

The oscillation frequency ω_{osc} produced from the CUT is considered to be an indirect parameter. An indirect parameter is a parameter which is not of interest in the

normal mode of the CUT and is evaluated only for test purposes. The tolerance limits of the indirect parameter ω_{osc} is called the tolerance band of the oscillation frequency ω_{osc}. The tolerance band of oscillation frequency ω_{osc} for each CUT is determined using a Monte Carlo analysis of the converted CUT taking into account the tolerance limits of all components (definition 2) and important technology parameters.

Definition 2: Tolerance Limits of a Component

The tolerance limits of a component C_k are its maximum variations that keep all circuit parameters within their tolerance limits.

Components are primitive elements of an analog circuit such as resistors, capacitors, transistor length or width, etc. which are adjusted by the designer to fix the circuit parameters. Tolerance limits of a component are normally greater than its variations due to the manufacturing process and is determined by the designer.

Definition 3: Fault Absolute Observability (AO)

The fault absolute observability of a component C_k using the parameter P_i is defined to be the sensitivity of the parameter P_i with respect to the variations of the component C_k.

Assuming the parameter P_i to be a function F of a set of components in the circuit under test

$$P_i = F(C_1, C_2, ..., C_k, ..., C_n) = \frac{N(C_1, C_2, ..., C_k, ..., C_n)}{D(C_1, C_2, ..., C_k, ..., C_n)} \quad (1)$$

where the C_k's are the various circuit components on which P_i depends. N and D are the nominator and denominator of the function F. The fault absolute observability of the component C_k is therefore calculated by the sensitivity. As the large deviation variations should be also considered, the incremental sensitivity formulation [19] is used.

$$AO_{C_k}^{P_i} = \rho_{C_k}^{P_i} = \frac{S_{C_k}^{P_i}}{1 + S_{C_k}^{D} \frac{\Delta C_k}{C_k}} \tag{2}$$

where $\rho_{C_k}^{P_i}$ is the incremental and $S_{C_k}^{P_i}$ is the differential sensitivity of the parameter P_i and $S_{C_k}^{D}$ is the differential sensitivity of the dominator D with respect to the component C_k. It should be noted that incremental sensitivity is an extension of differential sensitivity and is used when the component C_k is submitted to a large deviation.

In the case of the oscillation-test strategy, the only parameter which is used to test the CUT is the oscillation frequency ω_{osc}. Therefore, the AO of a fault in the component C_k using the oscillation frequency is given by

$$\omega_{osc} = F(C_1, C_2, ..., C_k, ..., C_n) = \frac{N(C_1, C_2, ..., C_k, ..., C_n)}{D(C_1, C_2, ..., C_k, ..., C_n)} \tag{3}$$

$$AO_{C_k}^{\omega_{osc}} = \rho_{C_k}^{\omega_{osc}} = \frac{S_{C_k}^{\omega_{osc}}}{1 + S_{C_k}^{D} \frac{\Delta C_k}{C_k}} \tag{4}$$

where $\rho_{C_k}^{\omega_{osc}}$ is the incremental and $S_{C_k}^{\omega_{osc}}$ is the differential sensitivity of the ω_{osc} and $S_{C_k}^{D}$ is the differential sensitivity of the dominator D with respect to the component C_k. To increase the observability of a defect in a component in the oscillation-test method, the sensitivity of the oscillation frequency with respect to that component should be increased. In other words, during the process of converting the CUT to an oscillator, the oscillator architecture must be chosen so as to ensure the maximum possible CUT component

contribution in determining the oscillation frequency. Where only one oscillator cannot guarantee desirable *AO* for all CUT components, more than one oscillator may be constructed from the CUT to increase the fault coverage.

Definition 4: Fault Relative Observability (RO)

Fault relative observability of the component C_k using the parameter P_i with respect to the parameter P_j is the ratio of the AO of parameter P_i with respect to component C_k to the AO of parameter P_j with respect to the same component.

The relative observability of a fault in the component C_k using the parameter P_i with respect to the parameter P_j is given by

$$RO_{P_j}^{P_i}\Big|_{C_k} = \frac{\rho_{C_k}^{P_i}}{\rho_{C_k}^{P_j}} \tag{5}$$

where $\rho_{C_k}^{P_i}$ is the incremental sensitivity of the P_i with respect to the component C_k and $\rho_{C_k}^{P_j}$ is that of the functional parameter P_j with respect to the same component. The definition of *RO* is useful where a limited number of parameters are used to test the CUT. In this case, the *RO* is the ratio of the sensitivity of the parameter P_i, which used to test the CUT, to the sensitivity of the parameter P_j, which is not used to test the CUT, with respect to the component C_k.

In the oscillation-test method, the only parameter employed to test the CUT is the oscillation frequency and therefore the relative observability of a fault in the component C_k using the oscillation frequency with respect to the parameter P_j is defined as

$$RO_{P_j}^{\omega_{osc}}\Big|_{C_k} = \frac{\rho_{C_k}^{\omega_{osc}}}{\rho_{C_k}^{P_j}} \tag{6}$$

If the fault relative observability of the component C_k with respect to the parameter P_j is greater than one, it can be concluded that the sensitivity of the ω_{osc} with respect to the component C_k is higher than the sensitivity of parameter P_j with respect to the same component. The *RO* of a component C_k may be calculated for ω_{osc} with respect to all circuit parameters.

Definition 5: Catastrophic Fault

A short or open circuit in the CUT is said to be a catastrophic or hard fault if it deviates at least one of the CUT functional parameters out of its tolerance limits (definition 2).

Catastrophic faults are introduced by random defects and result in failures in various components. They are provoked, for example, by dust particles on a photolitographic mask and cause either short and open circuits or large deviation of CUT parameters from their tolerance band such as width-to-length (W/L) ratio of a MOS transistor [12],[20]. Obviously, an open or short circuit that maintain all the CUT functional parameters within their tolerance band is not considered to be a fault.

Definition 6: Parametric Fault

Any soft variation of a component greater than its tolerance limits (definition 2) is considered to be a parametric or soft fault.

A soft variation of a component is not a parametric fault if it keeps all CUT functional parameters within their tolerance limits. Parametric faults are caused by statistical fluctuations in the manufacturing process or by dust particles on a photolitographic mask.

Definition 7: Detectable Fault

A parametric or catastrophic fault is said to be detectable if it deviates the oscillation frequency out of its tolerance band (definition 5).

Faults which do not turn the oscillation frequency away from its tolerance band are not detectable. In the oscillation-test method the deviation of the indirect parameter ω_{osc} from its tolerance band is employed to detect faults.

Definition 8: Undetectable Variation Limits of a Component

The limits of a soft variation in a component which maintain the oscillation frequency within its tolerance band is called the undetectable variation limits of that component.

The undetectable variation limits of a component should be compared to its tolerance limits (definition 2) to conclude how good a parametric fault in that component is detectable. *RO* provides the same information numerically.

Having described the necessary definitions to analyze the parametric and catastrophic fault coverage in analog circuits, we evaluate the capability of the oscillation-test to cover these type of faults. The introduced definitions are not limited to the oscillation-test and can be used to analyze the efficiency of any test solution for analog circuits.

3 Operational Amplifier Design and Modeling

Before introducing the test technique, important characteristics of the op-amp under test and its related frequency domain model are presented. Fig. 1 shows the schematic

representation of a classical two-stage CMOS operational amplifier that is considered as the CUT. The op-amp has been designed using the 1.2 μm CMOS process parameters from MITEL Semiconductor.

The total amplifier DC open-loop gain is given by:

$$a_V = \frac{g_{m2} g_{m8}}{(g_{ds5} + g_{ds6})(g_{ds7} + g_{ds8})} \tag{7}$$

where the channel conductances, g_m and g_{ds}, are defined as:

$$g_m = \frac{\partial i_D}{\partial v_{GS}}\Big|_{I_D} \equiv \sqrt{(2\mu_O C_{OX} W/L)|I_D|} \tag{8}$$

$$g_{ds} = \frac{\partial i_D}{\partial v_{BS}}\Big|_{I_D} \equiv I_D \lambda \tag{9}$$

in which, μ_O is the channel surface mobility, C_{OX} is the capacitance per unit area of the gate oxide, W and L are effective channel width and length receptively, and λ is the channel length modulation parameter of the transistor. I_D represents the quiescent current and is provided by M1 and M4 transistors and R_B.

As the op-amp is compensated, its transfer function can be approximated to a single pole transfer function given by:

$$a_V(s) = \frac{a_V}{1 - s/p_1} \tag{10}$$

in which p_1 represents its dominant pole. The unity-gain bandwidth of the op-amp is calculated as follows:

$$\omega_T = -a_V p_1 = g_{m1}/C_c \tag{11}$$

When the op-amp operates at high frequencies ($s/p_1 >> 1$) the transfer function is simplified to

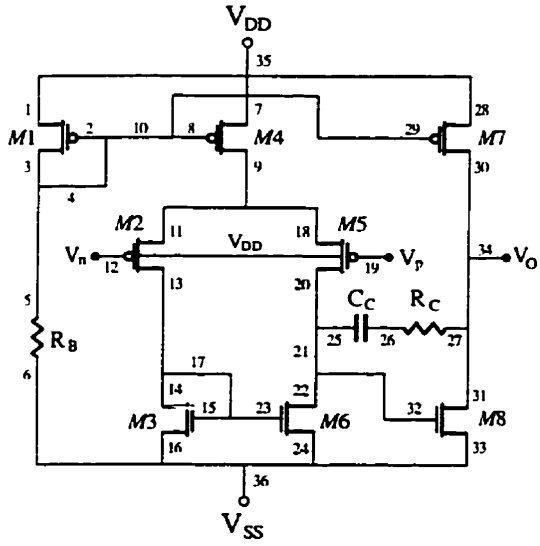

Fig. 1: Compensated CMOS operational amplifier.

$$a_V(s) = \frac{-a_V p_1}{s} \tag{12}$$

In the test-mode *TM*, the op-amp is separated from the original circuit and converted to an oscillator. A testable op-amp which offers this possibility is shown in Fig. 1. When the *TM* signal is active, the negative, positive, and output pins of the op-amp are separated from the original circuit using S_1, S_2, and S_3 switches respectively and will be available for the test structure. As the input impedance of an op-amp is generally very high, the S_1 and S_2 switches does not affect the op-amp characteristics and can be implemented using a simple minimum size transistor. The switch S_3 appears at the output of the op-amp and may affect the output impedance and the stability of the op-amp. Therefore it must be implemented using a CMOS switch to minimize the R_{ON} impedance [21],[22]. The testable op-amp has been designed using an N-well CMOS 1.2 μm technology and the area overhead related to switches comparing to the original op-amp active area is around 4%. It should be noted that the internal structure of the op-amp employed as the test vehicle in this paper is very simple and therefore the 4% area overhead can be considered

as the maximum area overhead and in general the area overhead is smaller. The layout of the testable op-amp is shown in Fig. 3. The frequency response of the testable op-amp is depicted in Fig. 4.

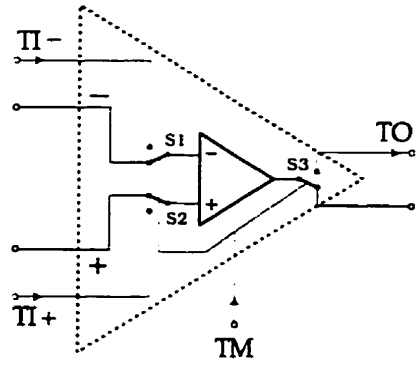

Fig. 2: Schematic representation of the testable op-amp.

Table 1: Important characteristics of the original and testable op-amp (C_L = 5 pF).

Parameter	Post-Layout Simulation Results (Original Opamp)	Post-Layout Simulation Results (Testable Opamp)
Unity-gain bandwidth (f_T)	28.8 MHz	26 MHz
Gain at dc (a_V)	91.6 dB	91.6 dB
Dominant pole (p_1)	4700 rad/s	4700 rad/s
Phase margin (φ_M)	87°	83°
Slew rate (SR)	> 110 V/μs	> 110 V/μs
Offset voltage (V_{OS})	5 μV	5 μV

Table 1 summarizes the important characteristics of the original and testable op-amps. The results were obtained from the extracted schematic of the op-amp's layout considering the parasitic capacitors and resistors in the presence of a 5 pF capacitive load.

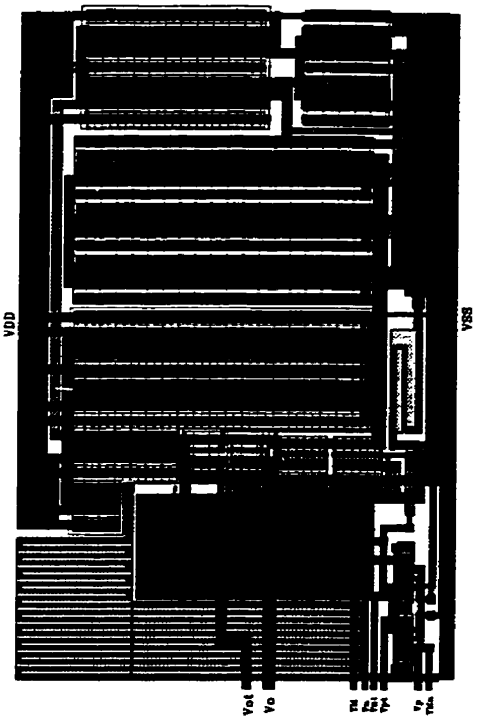

Fig. 3: Layout of the testable op-amp using the N-well CMOS 1.2μm technology of MITEL semiconductor.

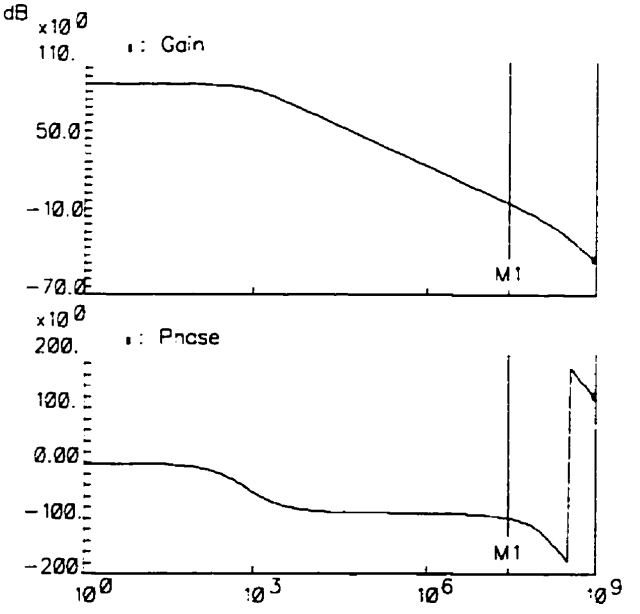

Fig. 4: AC response of the testable CMOS op-amp.

A suitable method to convert an analog building block to an oscillator consists of adding a feedback loop to its structure and then adjusting the feedback elements to establish and sustain oscillation. Depending on the CUT the feedback loop can be negative, positive or a combination. In the case where a single oscillation frequency is not sufficient to cover all target faults, a suitable element of the feedback may be varied to produce different oscillation frequencies. Different building blocks can be easily combined together to construct an oscillator whose oscillation frequency depends on the characteristics of the building blocks under test. In this paper, various design for testability techniques based on the above approaches are introduced to test op-amps.

4 Operational Amplifier Testing

In this section, DFT techniques based-on oscillation-test method are presented for single, double, and multiple op-amps. Many studies has been devoted to determine the dominant fault types and to define the appropriate fault models. Research results denote that 80-90 percent of observed analog faults were catastrophic faults consisting of shorts and opens in diodes, transistors, resistors and capacitances [23],[24]. It was also found that a test method which detects 100% of catastrophic faults did also find the majority of soft faults depending on the deviation value of the soft fault [20]. The occurrence probability of faults has been also considered [24] as presented in Table 2. As a conclusion the studies indicate that catastrophic faults and especially short faults are dominant in both bipolar and CMOS processing technologies. Therefore, a comprehensive list of catastrophic faults is inducted and simulated for all case studies. A set of parametric faults is also injected depending on the CUT.

Table 2: Classification of occurrence probability of faults in a CMOS technology [24].

Fault class	Device failures	Interconnect defect
More probable	Gate-drain short Gate-source short	Short between diffusion lines
Probable	Open on drain contact Open on Source contact	Aluminum polysilicon cross-over broken
Less probable	Gate-substrate short Open on gate contact	Short between Aluminum lines

In order to evaluate the testability of the proposed test techniques, the process of introducing an exhaustive list of shorts and opens at devices is used with five faults per transistor [12]. Faults such as circuit node opens and shorts between different nodes of the CUT are also injected. 36 different nodes are identified on the op-amp schematic. Note that some nodes that seem schematically redundant such as 6, 16, 24, 33, and 36 are not physically redundant. The total number of 658 faults, consisting of 28 open faults and 630 short faults ($C_2^{36} = 36!/(2!(36-2)!)$ is used as the fault dictionary for the op-amp under test. An open fault is simulated by introducing a 10 M ohm resistor. A short fault is modeled by a 10 ohm resistor.

4.1 Single Operational Amplifier DFT

Fig. 5 shows the schematic view of a single op-amp oscillator. The negative feedback loop consists of an RC delay and the positive feedback is a voltage divider. This oscillator employs both positive and negative feedback loops. To facilitate the mathematical analysis the combination of feedback loops is presented by a single negative feedback block in which the positive feedback appears as a term with negative sign. The feedback block converts the op-amp under test to a second order system which has the potential of oscillation. The new transfer function is derived as follows:

$$A_V(s) = \frac{a_V(s)}{1 + a_V(s)f(s)} \tag{13}$$

where,

$$f(s) = \frac{1}{1 - s/p_2} - G \tag{14}$$

in which $G = R_2/(R_1 + R_2)$ and $p_2 = -1/RC$. Substituting $a_V(s)$ and $f(s)$ in $A_V(s)$ we obtain

$$A_V(s) = \frac{a_V p_1 (p_2 - s)}{s^2 + (Ga_V p_1 - (p_1 + p_2))s + ((1 - G)a_V p_1 p_2 + p_1 p_2)} \tag{15}$$

In order to construct the oscillator from this new transfer function, its poles must be placed on the imaginary axis in the s domain. The poles are obtained by equating to zero the denominator of the new transfer function. Therefore, the coefficient of the s term must be forced to zero by proper selection of the value of G, which results in:

$$G = \frac{p_1 + p_2}{a_V p_1} \tag{16}$$

The natural oscillation frequency for the new system is given by

$$\omega_{osc}{}^2 = (1 - G)a_V p_1 p_2 + p_1 p_2 = a_V p_1 p_2 - p_2{}^2 \tag{17}$$

The differential sensitivity of the oscillation frequency with respect to a_V and p_1 is therefore given by

$$S_{a_V}^{\omega_{osc}} = \frac{p_1 p_2}{2\sqrt{a_V p_1 p_2 - p_2{}^2}} \tag{18}$$

$$S_{p_1}^{\omega_{osc}} = \frac{a_V p_2}{2\sqrt{a_V p_1 p_2 - p_2{}^2}} \tag{19}$$

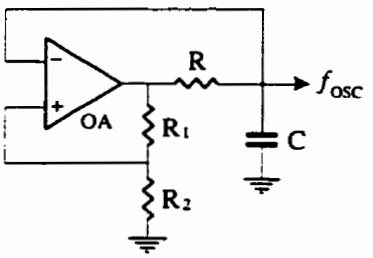

Fig. 5: Single op-amp oscillator. The nominal output frequency is chosen to be 5.8 MHz.

The maximum achievable frequency using this oscillator can be calculated by equating to zero the derivative of ω_{osc} with respect to p_2 which results in $p_2 = a_V p_1/2$ and $G \approx 0.5$ and therefore

$$\max\{\omega_{osc}\} = a_V p_1/2 \tag{20}$$

Based on equation (12) the maximum oscillation frequency (≈ 13 MHz) can be obtained by selecting RC = 1.23×10^{-8} (C = 1 pF and R = 12.3 KΩ) and $R_1 = R_2$. The absolute value of R_1 and R_2 can be small because only their ratio is important. However, very small resistor values increase the power consumption. The area overhead related to additional circuitry can be minimized by choosing the largest possible value for p_2 which minimizes the values of R and C. Note that the maximum limit of p_2 is $a_V p_1$.

In our experimentation a medium frequency has been produced by selecting RC = 10^{-7}. The positive feed-back of G ≈ 1/16 is necessary to establish sustained oscillations. The oscillation frequency, f_{osc}, obtained by simulation is approximately 5.8 MHz. This oscillation frequency depends strongly on important characteristics of the op-amp under test which are determined by all components of the op-amp. Faults in the op-amp will deviate its characteristics from their nominal value which can be monitored by observing the oscillation frequency.

As mentioned before, in this section, an exhaustive list of catastrophic faults is injected to quantify the fault coverage. In this particular case, the majority of injected faults have resulted in loss of oscillation. The tolerance band of the oscillation frequency has been determined using a Monte Carlo analysis of the oscillator taking into account the tolerance limits of all components and important technology parameters. Fig. 6 illustrates the result of Monte Carlo analysis. To visualize the results, the Fourier transform of the oscillation frequency is given. The remaining injected faults caused significant deviation of the oscillation frequency from its tolerance band. Table 3 presents the resulting oscillation frequencies for the faults which preserve the oscillations but deviate its frequency from its nominal value. Faults which result in the loss of oscillation are not presented in this table. Only one fault of each schematically redundant fault set is presented in the table. As the results demonstrate, all injected faults manifested themselves by affecting the oscillation frequency and therefore can be detected.

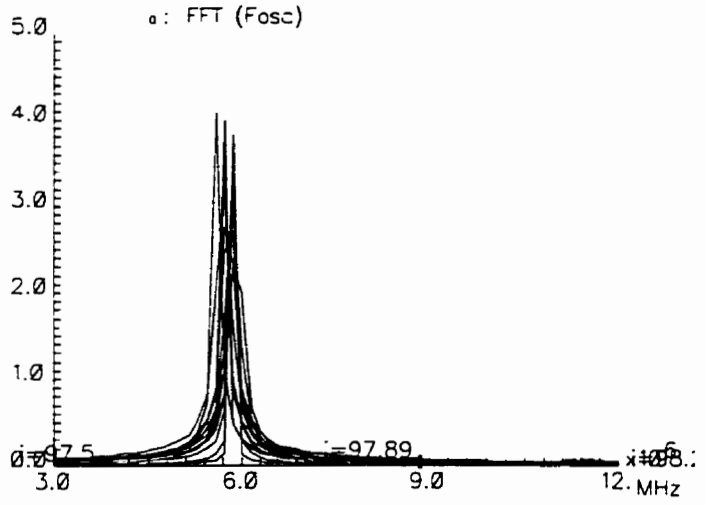

Fig. 6: Monte Carlo analysis of the Fourier transform of the single opamp oscillator's output signal. The tolerance band of the oscillation frequency is determined to be around [-5.5% , 4%].

Table 3: CMOS op-amp faults which maintain the oscillations

Fault	Output Voltage Level (V)	Oscillation Frequency
N7,9-S*	<-4.01 , 3.03>	$f_o \approx 1.2 f_{osc}$
N29,30-S*	<-2.47 , 2.8>	$f_o \approx 0.85 f_{osc}$
N26,27-S*	<-4.53 , 4.76>	$f_o \approx 0.86 f_{osc}$
N26-O*	<-4.63 , 4.72>	$f_o \approx 1.85 f_{osc}$
All Other Faults	***No Oscillation***	***No Oscillation***

N7,9-S: Short between nodes 7 and 9. N26-O: Open at node 26.

*: Representing a set of schematically redundant faults.

Another single op-amp sinusoidal oscillator, which employs both positive and negative feedbacks, is presented in Fig. 7. The op-amp is first converted to a limited-gain amplifier and then cascaded with a simple RC high-pass filter to construct a band-pass circuit. If the gain of the pass-band system is slightly greater than unity at its central frequency, connecting the output of the band-pass circuit to its input will result in sustained oscillations at its central frequency. In reality noise at the input of the system is band-pass filtered, slightly amplified, and then fed back to the input, and the same action is repeated. Therefore, the system tends to oscillate at its central frequency. The amplitude of oscillations is limited by non-linear properties of the op-amp. Note that, the higher the quality factor of the band-pass system, the purer the sinusoidal oscillation frequency.

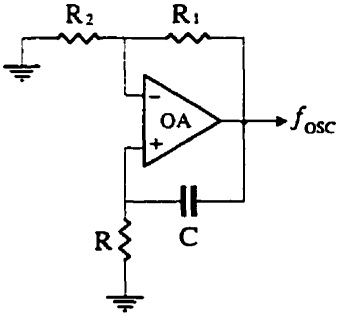

Fig. 7: Single-op-amp oscillator. The nominal output frequency is chosen to be 5.8 MHz.

In order to obtain the condition and the frequency of oscillation the same procedure employed for the previous oscillator is pursued. The new transfer function is given by $A_V(s)$ as described in the equation (9) where

$$f(s) = G - \left(\frac{-s/p_2}{1 - s/p_2} \right) \tag{21}$$

in which $G = R_2/(R_1 + R_2)$ and $p_2 = -1/RC$. Substituting $a_v(s)$ and $f(s)$ in $A_V(s)$ we get

$$A_V(s) = \frac{a_V p_1 (p_2 - s)}{s^2 + ((1-G)a_V p_1 - (p_1 + p_2))s + (Ga_V p_1 p_2 + p_1 p_2)} \tag{22}$$

In order to obtain sinusoidal oscillations the coefficient of the term s in the dominator must be forced to zero using proper selection of the value of G which results in:

$$G = 1 - \frac{p_1 + p_2}{a_V p_1} \tag{23}$$

The system oscillation frequency is given by:

$$\omega_{osc}^{\ 2} = Ga_V p_1 p_2 + p_1 p_2 = a_V p_1 p_2 - p_2^{\ 2} \tag{24}$$

The guidelines for the oscillator component value selection is the same as explained for the previous oscillator. The second oscillator is especially interesting because it can be also used to convert an inverting opamp based amplifier to an oscillator using only a simple RC circuit.

The equations (17) and (24) have been verified using the fabricated chip and the practical results are close to predicted theoretical oscillation frequencies. At high frequencies the oscillation frequency is also affected by the slew-rate of the op-amp and therefore should be considered.

4.2 Double Operational Amplifier DFT

An oscillator structure [25] which is suitable for testing two op-amps together is shown in Fig. 8. This oscillator is a simple sinusoidal oscillator using op-amps compensation poles and therefore its oscillation frequency depends tightly on the op-amps internal structure. This oscillator represents a smaller area overhead than previous oscillator.

Assuming p_2 = -1/RC and $a_{V_{OA_i}}(s) = -a_{V_{OA_i}} p_{OAi}/s$ (i = 1,2), the characteristic equation of the oscillator is given by

$$s^3 - p_2 s^2 + a_{V_{OA2}} p_{OA2} p_2 s - a_{V_{OA2}} p_{OA2} a_{V_{OA1}} p_{OA1} p_2 = 0 \tag{25}$$

Therefore, the condition of oscillation and the frequency of oscillation (ω_{OSC}) are found to be

$$p_2 = a_{V_{OA1}} p_{OA1} \tag{26}$$

$$\omega_{osc}^{\ 2} = a_{V_{OA1}} p_{OA1} a_{V_{OA2}} p_{OA2} \tag{27}$$

The term $a_{V_{OA_i}} p_{OAi}$ represents the unity-gain bandwidth of the ith op-amp (OAi). Therefore, the oscillation frequency is equal to the geometric mean of gain bandwidth of two op-amps. It depends equally on internal characteristics of both op-amps. As an example, the differential sensitivity of the oscillation frequency with respect to is given by

$$S_{a_{V_{OA1}}}^{\omega_{osc}} = \frac{1}{2}\sqrt{\frac{p_{OA1} p_{OA2} a_{V_{OA2}}}{a_{V_{OA1}}}} \tag{28}$$

To determine the tolerance band of the oscillation frequency in the test mode a Monte Carlo analysis taking into account the tolerance limits of all components and important technology parameters. The tolerance band of the oscillation frequency is determined to be [-4% , 5.7%]. The procedure of exhaustive catastrophic fault injection

and detection, as explained for single op-amp oscillator, has been exercised. The faults which cause a deviation of the oscillation frequency from its nominal value are shown in Table 4. As the faults which result in the loss of oscillation are very numerous, they are not presented in this table. To simplify the presentation, only one representing fault of each set of schematically redundant faults is presented in the table.

By a simple oscillation frequency evaluation process, only 4 faults remain undetectable because they do not cause the oscillation frequency to exit the tolerance band. Therefore, 4 faults out of 1316 (2×658) injected faults remain undetectable which results in a fault coverage of around 99%. It is interesting to note that the majority of faults which do not cause a significant deviation of the oscillation frequency from its nominal value can be detected by analyzing the voltage level of the oscillating signal.

4.3 Multiple Operational Amplifier DFT

An approach to speed up the test process and to reduce the area overhead is to place all existing op-amps in a chain and construct an oscillator with them. This is similar to scan-chain technique widely used in digital testing to verify flip-flops.

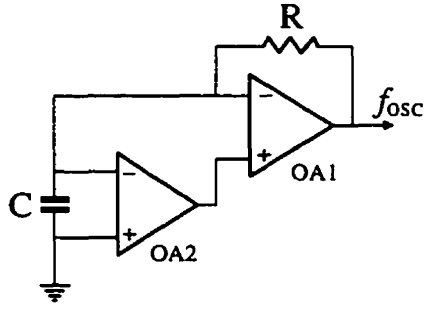

Fig. 8: A DFT technique to convert two op-amps to a sinusoidal oscillator.

Table 4: Comprehensive list of catastrophic faults in OA1 and OA2 which deviate the oscillation frequency.

Fault	Output Oscillation Frequency	Fault	Output Oscillation Frequency
OA1N1-O	$f_O \approx 1.49 f_{osc}$	OA2N3-O	$f_O \approx 1.01 f_{osc}$
OA1N3-O	$f_O \approx 1.50 f_{osc}$	OA2N12-O	$f_O \approx 1.04 f_{osc}$
OA1N14-O	$f_O \approx 0.6 f_{osc}$	OA2N14-O	$f_O \approx 1.04 f_{osc}$
OA1N14-O	$f_O \approx 0.7 f_{osc}$	OA2N5,7-S*	$f_O \approx 0.9 f_{osc}$
OA1N5,7-S*	$f_O \approx 1.59 f_{osc}$	OA2N27,28-S*	$f_O \approx 0.92 f_{osc}$
OA1N27,28-S*	$f_O \approx 1.26 f_{osc}$	OA2N5,18-S*	$f_O \approx 1.08 f_{osc}$
OA1N5,11-S*	$f_O \approx 1.39 f_{osc}$	OA2N24,25-S*	$f_O \approx 0.83 f_{osc}$
OA1N24,25-S*	$f_O \approx 0.76 f_{osc}$	OA2N24-O*	$f_O \approx 0.93 f_{osc}$
OA1N24-O*	$f_O \approx 2.23 f_{osc}$	**All Other Faults**	***No Oscillation***
OA2N1-O	$f_O \approx 1.01 f_{osc}$		

OA1N1-O: Open at the node 1 of the OA1, OA1N7,9-S: Short between nodes 7 and 9 of the OA1, *: Representing a set of schematically redundant faults.

The oscillator presented in Fig. 9 is an extension of the single op-amp oscillator presented in this paper. Increasing the number of op-amps in the loop decreases the oscillation frequency. Using this oscillator, several oscillation frequencies can be produced by varying the value of the resistor. Increasing the number of oscillation frequencies improves the fault detectability. This oscillator is feasible for more than two op-amps.

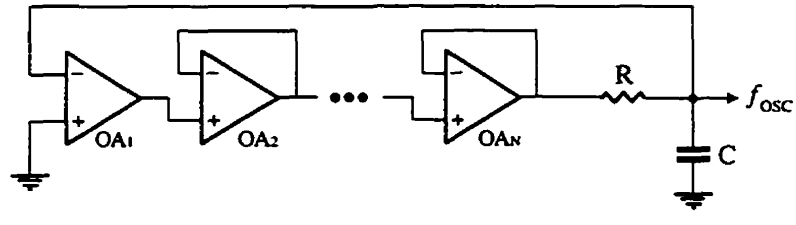

Fig. 9: Multiple op-amp phase-shift oscillator extended from single op-amp oscillator suitable for more than two op-amps (R= 1 KΩ and C = 1 pF).

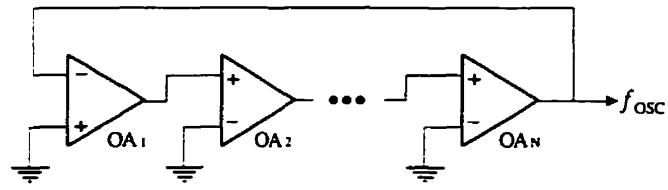

Fig. 10: Multiple op-amp ring oscillator suitable for more than two op-amps.

The oscillator introduced in Fig. 10 is a ring oscillator implemented using op-amps. The first op-amp is inverting and the rest are non-inverting. The oscillation period is equal to the sum of the delays introduced by op-amps and therefore it can be estimated by

$$f_{osc} = 1 \Big/ \sum_{i=1}^{N} (PD^{+}_{OAi} + PD^{-}_{OAi}) \tag{29}$$

where PD^{+}_{OAi} and PD^{-}_{OAi} represent the positive and negative propagation delays of ith op-amp respectively. As the op-amps operate as comparators in linear and non-linear region of the transfer function, the propagation delays must be determined using a large signal analysis. Propagation delay of an op-amp equals the sum of the delays of each stage. The delay for each stage is defined as the time it takes for its output voltage V_{SO} to make the transition from its quiescent state V_{QS} to the trip point V_{TRP} of the following stage. The trip voltage of a stage is approximated by the input voltage required for the current of its output switching transistor (in saturation) to equal the bias current of the transistor. The propagation delay of each stage can be characterized by

$$PD_{S_N} = (V_{QS_N} - V_{TRP_{N+1}}) \frac{C_{T_N}}{I_{SS_N}} \tag{30}$$

where C_T represent the sum of charge, parasitic, and compensation capacitances seen at the output of the stage and I_{SS} is the current available to charge or discharge the capacitance C_T. More details about the estimation of the propagation delay and transistor-

level analysis is found in [21]. It can be concluded that the propagation delay contributed by each op-amp depends on all its internal components and therefore the propagation delay has the potential of fault detection.

To evaluate the fault coverage of the proposed multiple op-amp test techniques, a complete analog signal processing unit consisting of 8 op-amps has been chosen as the test vehicle. Both multiple op-amp test schemes have been implemented and the fault coverage has been analyzed using an exhaustive list of catastrophic faults. It should be noted that, in both test structures the op-amps are position independent, except OA_1 in Fig. 9, and contribute equally in the oscillation frequency. In the other words, all op-amps affect similarly the oscillation frequency regardless of their position. Therefore, injecting all possible faults in a representing op-amp to quantify the fault coverage would be sufficient. To verify this assumption, the faults have been also inducted in another op-amp and similar results have been obtained.

The fault simulation results are presented in Table 5. The results of Monte Carlo analysis to determine the tolerance band of the oscillation frequency for each DFT structure are also presented in the same table. For the sake of simplicity, the faults which cause loss of oscillation are not included in the table. As the results indicate, the fault sensitivity of the ring oscillator is slightly higher than that of the phase shift oscillator.

For the ring oscillator, the oscillation frequency of only one fault, which represents 4 physically different faults out of possible 658, remains in the tolerance band. Therefore the fault coverage is about 99 %. For the phase shift oscillator structure, 3 faults, which represent 53 physically different faults, do not exit the oscillation frequency from its tolerance band resulting in a fault coverage of 92 %. As it will be explained further in this paper, this difference comes from the fact that the op-amps are converted to unity-gain

amplifiers in the phase-shift oscillator, which decreases the sensitivity to the op-amp's characteristics. The discrete fast Fourier transform (FFT) of the output oscillating signal without fault and in the presence of a fault (N5,6-S) that only deviate the oscillation frequency from its nominal value is illustrated in Fig. 11. Our experimentation indicate that there is a compromise between the number of op-amps in the loop and the fault coverage. As the number of op-amps in the loop increases the fault coverage decrease. Therefore a compromise should be done between the number of op-amps in the loop and the desired fault coverage.

Table 5: Comprehensive list of catastrophic faults in multiple op-amp ring and phase-shift oscillators.

Ring Oscillator (Fig. 10) Tolerance Band: [0.95 f_{osc}, 1.065 f_{osc}]		**Phase-Shift Oscillator (Fig. 9) Tolerance Band: [0.94 f_{osc}, 1.045 f_{osc}]**	
Fault	**Output Oscillation Frequency**	**Fault**	**Output Oscillation Frequency**
N1-O	$f_O \approx 1.13\, f_{osc}$	N1-O	$f_O \approx 0.91\, f_{osc}$
N3-O	$f_O \approx 1.12\, f_{osc}$	N3-O	$f_O \approx 0.91\, f_{osc}$
N26-O	$f_O \approx 1.15\, f_{osc}$	N26-O	$f_O \approx 1.15\, f_{osc}$
N5,13-S*	$f_O \approx 1.15\, f_{osc}$	N5,13-S*	$f_O \approx 0.90\, f_{osc}$
N5,6-S*	$f_O \approx 1.13\, f_{osc}$	N5,6-S*	$f_O \approx 0.92\, f_{osc}$
N7,9-S*	$f_O \approx 1.14\, f_{osc}$	N7,9-S*	$f_O \approx 0.90\, f_{osc}$
N8,9-S*	$f_O \approx 0.91\, f_{osc}$	N8,9-S*	$f_O \approx 0.93\, f_{osc}$
N26,27-S*	$f_O \approx 0.94\, f_{osc}$	N26,27-S*	$f_O \approx 0.95\, f_{osc}$
N29,30-S*	$f_O \approx 0.91\, f_{osc}$	N29,30-S*	$f_O \approx 0.93\, f_{osc}$
All Other Faults	***No Oscillation***	**All Other Faults**	***No Oscillation***

N1-O: Open at the node 1 of the op-amp, N6,8-S: Short between nodes 6 and 8 of the op-amp, *: Representing a set of schematically redundant faults.

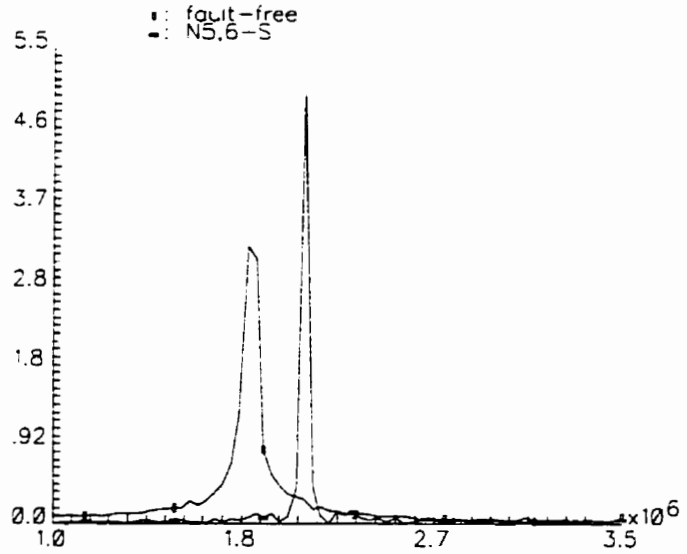

Fig. 11: FFT of the output signal of the ring oscillator-based test structure without and in the presence of a fault that cause a small deviation of the output frequency.

5 Process Variation Consideration

Oscillation-test methodology has the potential of measuring precisely different characteristics of the CUT. In the following we present a technique for gain-bandwidth measurement of op-amps that can be used either as an on-chip test technique or as a low-cost off-chip method. In fact as the equations (17) and (24) imply, the proposed DFT techniques for single op-amp in section 4.1 can be directly used as a technique to measure the op-amp gain-bandwidth ($a_V p_1$) as follows.

$$a_V p_1 = \frac{\omega_{osc}^{\ 2} + p_2^{\ 2}}{p_2} \tag{31}$$

Therefore, knowing p_2 and measuring ω_{osc}, the op-amp's gain-bandwidth can be deducted. The drawback of this technique for on-chip measurement is the tolerance of the p_2 which is determined by R and C. To overcome this problem we propose to perform two different oscillation frequency measurements.

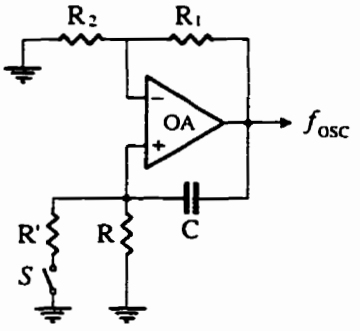

Fig. 12: Measurement set-up for op-amp's gain bandwidth.

As shown in Fig. 12, the first oscillation frequency measurement is performed when the switch S is off and the same measurement is repeated when the switch S is close. The first oscillation frequency denoted by ω_{osc} and the second oscillation frequency represented by ω'_{osc}, are given by

$$\omega_{osc}^{\ 2} = a_V p_1 p_2 - p_2^{\ 2} \tag{32}$$

$$\omega'^{\ 2}_{osc} = a_V p_1 p'_2 - p'^{\ 2}_2 \tag{33}$$

where $R' = kR$, $p_2 = -\dfrac{1}{RC}$ and therefore

$$p'_2 = -\frac{R+R'}{RR'C} = -\left(\frac{k+1}{k}\right)\frac{1}{RC} = Kp_2 \tag{34}$$

Using relationships (32), (33) and (34), the gain bandwidth of the op-amp can be calculated as

$$a_V p_1 = \frac{\left(K^2 - K\right)\left(K^2\omega_{osc}^{\ 2} - \omega'^{\ 2}_{osc}\right)}{\sqrt{K\omega_{osc}^{\ 2} - \omega'^{\ 2}_{osc}}} \tag{35}$$

where ω_{osc} and ω'_{osc} are directly measured and K is a ratio parameter and not a resistor or capacitor value and therefore much less susceptible to process variations.

6 Practical Considerations and Discussion

In this section some practical considerations and guidelines for successful and efficient implementation of the proposed test techniques are discussed.

6.1 Analog switches

Switches are the key components in analog testing and provide the programmability of the test structure. The accuracy of the switches directly affects the accuracy, and therefore the functionality, of the test system, especially when we deal with low-voltage signals and where high measurement precision is sought. Due to its non-ideal characteristics, it may cause serious performance degradation of the circuit under test. The most important characteristics of a switch are its on and off resistances (R_{ON} and R_{OFF}) and the values of its parasitic capacitors.

The R_{ON} and R_{OFF} values affect the transparency of the switches in the test structure. For switches to be transparent in the CUT and not degrade its performance, their R_{ON} must be as low as possible and their R_{OFF} must be as high as possible.

The R_{ON} of a MOS switch and its thermal noise contribution can be reduced by increasing the W/L ratio. The $1/f$ noise contribution of MOS switches can be reduced by increasing their W and L. Increasing W and L arbitrarily increases the parasitic capacitor values and consequently increases the feedthrough effect. A compromise must therefore be made to satisfy all requirements.

Parasitic capacitors determine the clock feedthrough and charge injection error values introduced by the switch. To minimize the clock feedthrough error, the parasitic capacitors must be as low as possible. Using a CMOS switch or a dummy transistor and a symmetrical switching procedure, feedthrough error can be diminished through

cancellation [21]. Careless design of test switches may cause instability problems in critical designs due to the presence of parasitic capacitors.

In the test structures presented in this paper, the switches can be divided into two main categories depending on their application: 1) switches appearing in the signal path of the CUT, such as switches which divide the CUT into building blocks, and 2) switches which are not inserted in the signal path, like switches used to establish feedback loops. The first category of switches must be realized using CMOS switches to minimize R_{ON}. Reducing R_{ON} decreases the degradation of the signal amplitude and reduces the instability problems. As no precision voltage measurement is required in this test method and clock feedthrough has no effect on the test performance, the second category of switches can be realized simply using a minimum-sized NMOS transistor.

Another problem related to test switches is their testability. It may happen that a fault in a test switch cause that the CUT be permanently in the test mode. Therefore, in the test mode the CUT passes the test but it does not perform its function in the normal mode as it is permanently in the test mode due to the test switch malfunction. Our solution to this problem for the proposed design for testability techniques consists of opening and closing the test switch and observing the oscillation frequency. If the CUT oscillates whatever the state of the test switch, the test switch is faulty because the CUT is always in the test mode. If the CUT does not oscillate in both modes, either the test switch or the CUT is faulty. Finally, if the CUT oscillates only in the test mode, the test switch is fault-free. Therefore, situations such as the oscillation of the CUT in its normal mode will be detected by verifying test switches.

6.2 Effect of Noise

The equivalent RMS noise of the CUT is normally much smaller than the amplitude of the oscillation signal and therefore cannot affect its frequency. If the equivalent RMS noise is considerable, it may only cause a small jitter in the oscillation signal. In practice, many oscillation cycles are used to estimate the oscillation frequency, and consequently the jitter is averaged and due to the random nature of noise is canceled. However, if the oscillation signal amplitude is as small as the CUT equivalent RMS noise, which is much far from the case in practice, the oscillation frequency will be seriously affected by the noise.

6.3 Fault Coverage

For all case studies presented in this paper, a comprehensive list of hard faults has been inducted and the oscillation frequencies have been analyzed. The results confirm that a high fault coverage can be achieved by only output frequency evaluation for all cases.

The reasons for this fault coverage resides in three facts:

1. Operational amplifiers have at least two stages of amplification which results in a very high gain. In the majority of applications, a feedback loop is added to establish the gain to a small but stable value which causes the redundancy in the op-amp-based analog circuits. In that case, the faults which decrease the open loop gain by a factor of 2, for example, will not affect the op-amp-based circuit performance. In the test structures presented in this paper the oscillation frequency depends directly on the intrinsic characteristics of the op-amps and therefore such kinds of faults can be monitored.
2. There are four sources of imprecision in analog testing: the imprecision related to the analog test vectors, the acceptable tolerance of the CUT, the imprecision of voltage

buffers, and noise. During the test process the acceptable performance deviation range must be enlarged to accommodate these sources of error because they may exist even if the CUT is fault free. In the oscillation-test based test structures, the test vector error is eliminated because no test stimulus is applied. The voltage buffer imprecision is also minimized, because the reference value is normally a frequency, rather than a voltage, which is easily transferable by buffers to where it can be converted to a number without significant precision degradation. Noise, in both voltage and time domains, is reduced by integrating over an arbitrary long period of time.

3. In a given oscillator, the oscillation frequency depends on a wide range of the AC behavior of its transfer function with variable sensitivities. For example, in a band-pass based oscillator the oscillation frequency depends on the entire range of its open-loop AC behavior having greater than unity gain. In fact, the oscillation frequency can be considered as the sum of frequency components which can pass through the band-pass system with an amplification. Therefore a change in any of this components will affect the oscillation frequency. When testing this band-pass system with a specified test frequency, based on conventional test methods, reliable information about the AC behavior of the rest of the transfer function can not be achieved. In practice, many test frequencies should be applied to assure a complete coverage over the AC behavior of the CUT. The sum of these test frequencies can be applied to the band-pass system as a multitone test frequency. In this case the AC behavior coverage is comparable to the coverage obtained by the evaluation of the oscillation frequency in oscillation-test strategy.

The reported results indicate that the fault coverage can be increased by simultaneous frequency and voltage level value evaluation of the output oscillation frequency or applying Fourier transform technique to analyze the output oscillating signal. As the fault coverage achieved by only oscillation frequency evaluation is satisfactory, the evaluation of the output voltage level has not found to be necessary.

7 Experimental Results

A test chip has been fabricated using 1.2 μm CMOS technology of MITEL Semiconductor which includes the operational amplifier and the test circuitry. The chip has been successfully tested. The gain bandwidth of the opamp has been measured using conventional measurement techniques and the approach presented in this paper and the mismatch between the results is less than 2.5% for all fabricated chips. Fig. 13 illustrates the photomicrograph of the fabricated chip. A typical output of the opamp in the test mode is illustrated in Fig. 14.

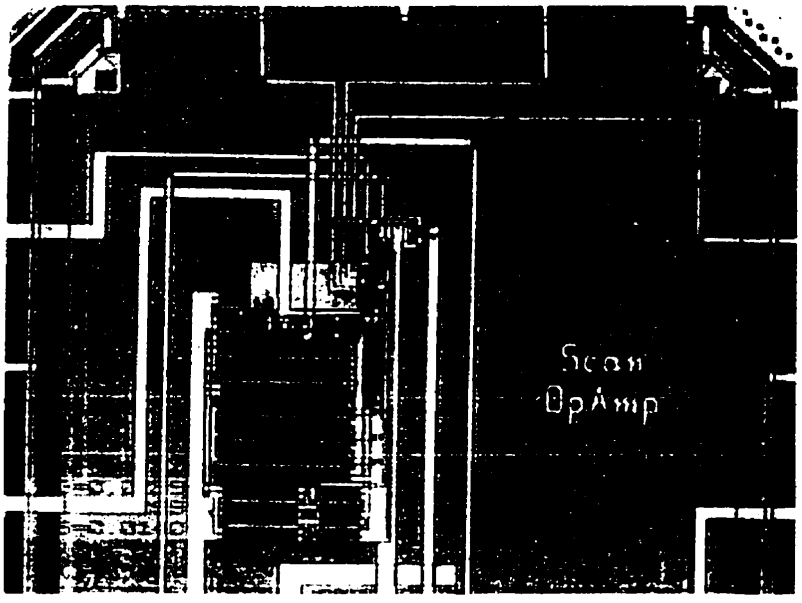

Fig. 13: Photomicrograph of the fabricated chip which includes a testable opamp.

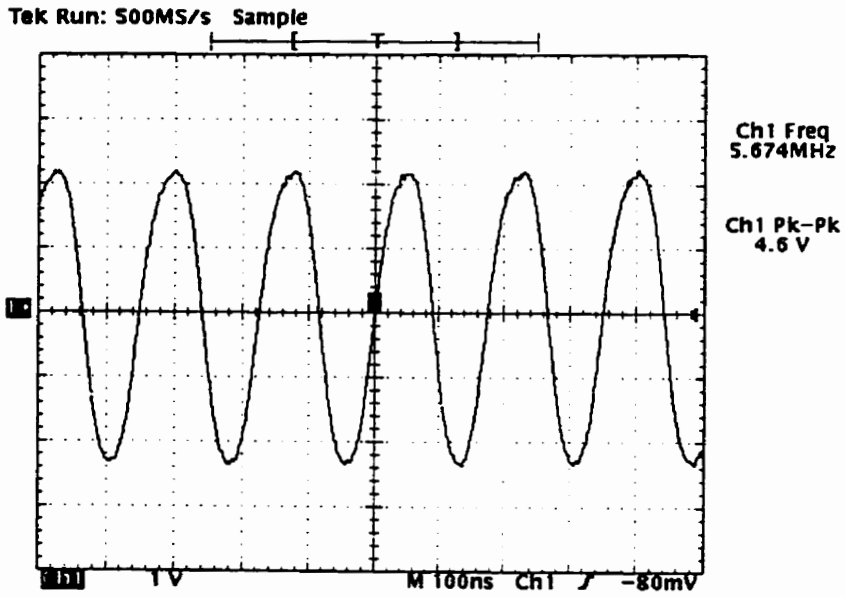

Fig. 14: A typical output of the fabricated operational amplifier incorporated in an oscillator in the test mode.

7 Conclusion

A new vector-less dynamic test strategy based on converting the CUT to an oscillator has been applied to op-amps. The advantages of the presented test techniques include a high fault coverage, reduced test time, very simple test procedure, and elimination of the test vector process. This test technique eliminates the need for costly specification tests and may be considered as a low-cost test method because no complicated circuit overhead is required. The results show that a multiple op-amp ring oscillator test technique can incorporate all existing op-amps on the chip and can achieve high fault coverage by analyzing only a single oscillation frequency. Demonstrated results confirm the robustness of the oscillation-test strategy for op-amps. The proposed test techniques can be practically integrated in a BIST structure and the oscillation frequency, which can be considered as a digital signal, can be easily interfaced to boundary scan or other test

methods dedicated to the logic part of the chip under test. Detectability of parametric faults using the presented DFT techniques is under investigation. Preliminary results show the potential of the proposed tests to cover parametric faults.

References

[1] Wey, C.-L, "Built-In Self-Test Structure for Analog Circuit Fault Diagnosis," *IEEE Transactions on Instrumentation and Measurement*, vol. 39, no. 3, 1990, pp. 517-521.

[2] Milor, L. and A.S. Vincentelli, "Optimal Test Set Design for Analog Circuits," Proc. of the *IEEE ICCAD*, 1990, pp. 294-297.

[3] Fasang, P.P., D. Mulins, and T. Wong, "Design for Testability for Mixed Analog/Digital ASICS," Proc. of the *IEEE Custom Integrated Circuit Conf.*, 1988, pp. 16.5.1-16.5.4.

[4] Wagner, K.D., and T.W. Wiliams, "Design for Testability of Mixed Signal Integrated Circuits," Proc. of the *IEEE Int'l Test Conf., 1988*, pp. 823-829.

[5] Marlett, M.J., and J.A. Abraham, "DC IATP-An-Iterative Analog Circuit Test Generation Program for Generating Single Pattern Tests," Proc. of the *IEEE Int'l Test Conf.*, 1988, pp. 839-844.

[6] Devarayanadurg, G., and M. Soma, "Analytical Fault Modeling and Static Test Generation for Analog ICs," Proc. of the *IEEE ICCAD*, 1994, pp. 44-47.

[7] Gielen, G., Z. Wang, and W. Sansen, "Fault Detection and Input Stimulus Determination for the Testing of Analog Integrated Circuits Based on Power-Supply Current Monitoring," Proc. of the *IEEE ICCAD*, 1994, pp. 495-498.

[8] Nigh, P., and W. Maly, "Test Generation for Current Testing," *IEEE Design & Test of Computers*, vol. 7, no.2, 1990, pp. 26-38.

[9] A'ain, A.K.B., A.H. Bratt, and A.P. Dorey, "Testing Analog Circuits by Power Supply Voltage Control," *Electronic Letters*, vol. 30, no. 3, 1994, pp. 214-215.

[10] Dorey, A.P., and J.B. Hibbert, "Simplified Test Strategies for Analog ICs," Proc. of the *European Test Conf.*, 1991, p. 494.

[11] Roca, M., and A. Rubio, "Selftesting CMOS Operational Amplifier," *Electronic Letters*, vol. 28, no. 15, 1992, pp. 1452-1454.

[12] Milor, L., and V. Visvanathan, "Detection of Catastrophic Faults in Analog Integrated Circuits," *IEEE Trans. on Computer Aided design*, vol. 8, no. 2, 1989, pp. 114-130.

[13] Soma, M. "Fault Coverage of DC Parametric Tests for Embedded Analog Amplifiers," Proc. of the *IEEE Int'l Test Conf.*, 1993, pp. 566-573.

[14] Renovell, M., F. Azais, and Y. Bertrand, "A Design for Test Technique for Multi-Stage Analog Circuits," Proc. of the *Asian Test Symposium*, 1995, pp. 113-119.

[15] Arabi, K. and B. Kaminska, " Parametric and Catastrophic Fault Coverage of Analog Circuits Using Oscillation-Test Methodology," Proc. of the *IEEE VLSI Test Symp.*, Monterey, April 1997, pp. 166-171.

[16] Arabi, K., and B. Kaminska, "Oscillation-Test Strategy for Analog and Mixed-Signal Integrated Circuits," Proc. of the *IEEE VLSI Test Symp.*, 1996, pp. 476-482.

[17] Arabi, K., B. Kaminska, and S. Sunter "Testing Integrated Operational Amplifiers Based on Oscillation-Test Method," Proc. of the 2nd *IEEE Int'l Mixed-Signal Testing Workshop*, May 1996, Quebec City, pp. 227-232.

[18] Arabi, K., and B. Kaminska, "Design for Testability of Integrated Operational Amplifiers Using Oscillation-Test Strategy," Proc. of the *IEEE ICCD*, Oct. 1996, Austin, pp. 40-45.

[19] Filder, J.K., "Differential-Incremental-Sensitivity Relationships," *Electronic Letters*, vol. 20, no. 10, 1984, pp. 626-627.

[20] Ohletz, M.J., "Hybrid Built-In Self-Test (HBIST) Structure for Mixed Analog/Digital Integrated Circuits," Proc. of the *2nd European Test Conference*, 1991, pp. 307-316.

[21] Allen, P., and D.R. Holberg, "CMOS Analog Circuit Design," *Holt, Rineheart and Winston*, 1987.

[22] Arabi, K., B. Kaminska, and J. Rzeszut, "BIST for Digital-to-Analog and Analog-to-Digital Converters," *IEEE Design & Test of Computers*, Fall 1996, pp. 40-49.

[23] Stapper, C., F. Armstrong, and K. Saji, "Integrated Circuit Yield Statistics," *Proc. IEEE*, vol. 71, 1983, pp. 453-470.

[24] Banerjee, P., and J.A. Abraham, "Fault Characterization of VLSI MOS Circuits," *IEEE Int. Conf. Circuits and Computers*, 1982, pp. 564-568.

[25] Senani R., "Simple Sinusoidal Oscillator Using Op-amp Compensation Poles," *Electronic Letters*, vol. 29, no. 5, 1993, pp. 452-453.

CHAPITRE 4

VÉRIFICATION DES INTERFACES BIOÉLECTRONIQUES DES SYSTÈMES IMPLANTABLES

4.1 Résumé

Les expériences cliniques des derniers 20 ans avec les systèmes implantables ont démontrées que les problèmes mécaniques des interfaces bioélectroniques et le changement d'état du tissu stimulé sont des causes importantes de mauvais fonctionnement de ces systèmes. Dans les chapitres précédents de cette thèse, le problème de testabilité des circuits électroniques des systèmes implantables a été étudié. Dans ce chapitre, nous allons aborder la testabilité des électrodes, les fils d'interconnexion et l'état du tissu qui est situé entre les électrodes.

4.2 "Monitoring the Electrode and Lead Failures in Implanted Microstimulators and Sensors"

Afin de vérifier l'état de l'interface bioélectronique et celui du tissu situé entre les électrodes, nous allons développer des techniques de monitoring permettant au médecin de modifier les paramètres ou la configuration du système implanté en fonction de résultat du test.

D'abord, nous présentons une technique de monitoring qui peut être appliquée à tous les systèmes implantables pour vérifier l'état des interfaces bioélectroniques. Ensuite,

des techniques spécifiques, dédiées à différentes applications seront développées. Ces techniques permettront un monitoring plus efficace et une surface additionnelle plus petite.

Ce travail a été soumis pour publication dans *IEEE Transactions on Rehabilitation Engineering*.

Monitoring the Electrode and Lead Failures in Implanted Microstimulators and Sensors

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Abstract

The electrodes and wire lead failures are between the main reasons of an implantable system malfunction. The impedance change and fibrosis of the living tissue which is in direct contact with the electrode are also important parameters to monitor. Measuring the resistance of leads, electrode-tissue contact and the interelectrode tissue can be used to verify the functionality of implanted electrodes and to deduce the state of the interelectrode tissue. This paper describes the feasibility of using an oscillator, the frequency of which is controlled by the above mentioned resistance, to test the electrode functionality as well as the state of the living tissue. It is shown that this approach results in a very low-cost and practical solution. The oscillator has been designed using CMOS 1.2μm technology parameters of MITEL semiconductor. The oscillator has been also

realized and evaluated using discrete components and in-vitro tests has been successfully performed using monopolar and bipolar cuff electrodes.

Two dedicated techniques have also been proposed for microstimulators and sensors. These techniques result in a lower silicon area. The presented monitoring scheme for microstimulators can verify the electrode and leads functionality without interrupting the stimulation procedure. Proposed techniques can be easily implemented in any implantable system to increase its reliability.

1 Introduction

There is a growing interest in implantable microstimulators and sensors in many therapeutic applications. Several implants have been designed for neuromuscular stimulation applications [1]-[3]. Current applications include implantable cardioverters and defibrillators, neuromuscular stimulators, bone growth stimulators, etc. Presently, more than 1.5 million peoples have pacemakers implanted worldwide [4]. Various implantable systems for medical measurement and diagnostic biotelemetry have been also reported in literature [5]-[9].

The implanted electrodes and connecting wires are submitted to corrosion and frequent stress due to the relative motion of the different muscle groups. It is well known that one of the most encountered problem causing the malfunction of implantable systems is the mechanical problem related to implanted electrodes and wire leads called also bioelectronic interface. It is also clinically important to monitor the state of the tissue which is in direct contact with the implanted electrode. It helps to optimize the stimulation parameters and to prevent the tissue damage. Unfortunately, the majority of the reported implantable devices has no means to detect such kind of problems.

The aim of this work is to develop simple and efficient techniques to verify the functionality of electrodes and leads after implantation. The interelectrode impedance is also monitored to verify the state of the tissue and the fibrosis. The obtained data can be used in the implant or be sent out to physician.

The proposed techniques are based on impedance measurement in which the equivalent impedance leads, electrode, and interelectrode tissue is used to detect faults or anomalies in the contacting living tissue. In the main proposed technique, a new test method for analog and mixed-signal circuits called oscillation-test strategy [10] is used. Oscillation-test forms an oscillator from the circuit under test (CUT) and evaluates the resulted oscillation frequency to detect faults.

The rest of this paper is organized as follows. A simplified model of the bioelectronic interface of implantable systems widely used in the literature along with a fault model is presented in section 2. Section 3 introduces an approach to monitor the functionality of electrode and leads in both implanted microstimulators and sensors. Customized techniques to test the bioelectronic interface of implantable devices are presented in section 4.

2 Electrode-Tissue Interface and Fault Modeling

The electrical conduction in a biological tissue is established by ion transfer in electrolytic environment. In contrary, in a metal wire the electrical conduction is formed by electron movement. Therefore, application of an electrical current to a biological tissue requires the conversion of electronic conduction to ionic conduction which is done by a process of energy conversion.

When an electrical current passes through an electrode-electrolyte interface, it forms an electrical field resulting from ion diffusion at the contacting surface between two environments. This capacitive region called also Helmholtz layer opposes the current injected and is predominant for currents injected at very low frequencies [11],[12].

The formation of an electrostatic layer and the presence of a diffusion layer are two principal processes that explain the behavior of the electrode-tissue interface. By neglecting the ionic diffusion, the electrical model of the electrode-tissue interface consists of a resistor R_t and a capacitor C_H in parallel as shown in Fig. 1.

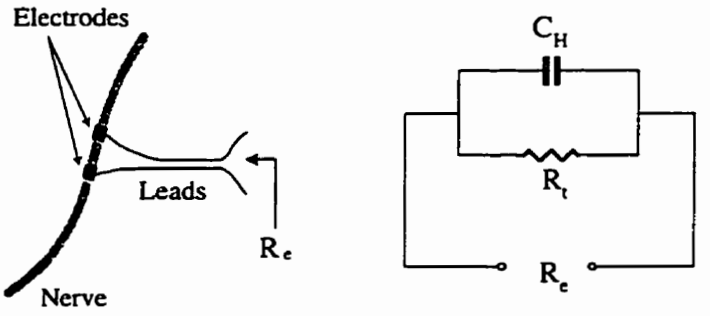


Fig. 1: Simplified electrical model of electrode-tissue interface.

The resistor R_t is the result of different current conduction behaviors at the electrode and tissue interface (electrons in the metal and ions in the living tissue). The capacitor C_H is formed due a layer of water molecules absorbed by the metal surface. C_H varies between 10 to 20 $\mu F/cm^2$ [11]. Taking into account the ionic diffusion process, two passive elements forming the Warburg equivalent impedance should be added to the simplified model [12] as shown in Fig. 2.

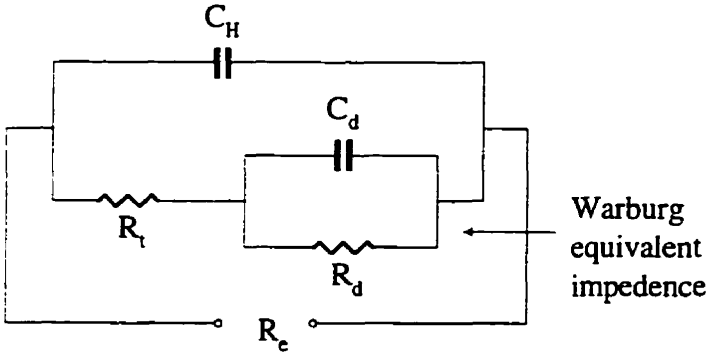


Fig. 2: Detailed electrical model of electrode-tissue interface.

For most of applications considering the contact resistance between the electrode and the tissue and modeling the tissue resistance by a parallel combination of a resistor and a capacitor [13] are sufficient and provide adequate accuracy. Depending on the electrode design, the tissue, and the application a nominal value can be defined for the equivalent impedance of the tissue and electrode-tissue contact. In most applications, in the normal condition, this impedance varies between 1 kΩ to 3 kΩ.

In order to detect faults and to characterize the state of the living tissue which is in contact with electrode, we propose to measure this impedance by inserting it in an oscillator and evaluating the oscillation frequency to detect faults.

Three kinds of impedance variations can be considered:

1) Very high impedance which represents the breakage of wire leads or electrodes or their complete corrosion.

2) Very low impedance which may be caused by short circuit between electrodes or leads created by mechanical contact or body fluids containing electrolytes and organic compounds.

3) Parametric impedance variations induced by a change in the state of the interelectrode tissue and the fibrotic encapsulation of the electrodes.

3 Unified Monitoring Approach

In this section, we introduce a universal technique to monitor the functionality of electrode and leads in both microstimulators and sensors. This technique is universal in the sense that it can be applied to various types of implantable devices regardless of their actual architecture.

3.1 Basic Principle

The basic principle to monitor the state of the electrodes, wire leads, and contacting tissue, which are in series together, consists of incorporating them in a simple oscillator as an element controlling the oscillation frequency by its impedance. The oscillation frequency related to this impedance is defined to be the nominal oscillation frequency. The deviation of the oscillation frequency from this nominal value indicates a variation of the equivalent impedance from its nominal value. As mentioned before, deviation of the equivalent impedance from its nominal value may represent the breakage of wire leads or electrodes or their complete corrosion, short circuit between electrodes or leads, or change in the state of the interelectrode tissue.

The impedance variations produce changes of the oscillation frequency which can be easily transmitted to the external controller or be treated by the implant. Oscillation frequencies around 50 kHz were chosen for the oscillator to prevent neuromuscular responses and electrode polarization effects.

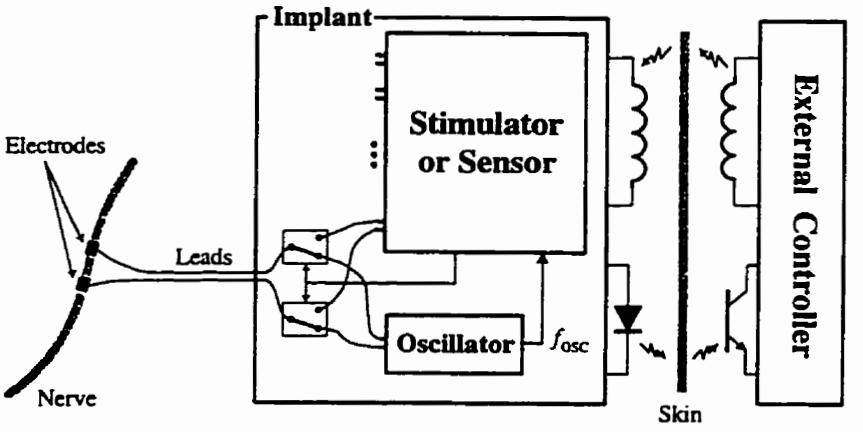


Fig. 3: Simplified block diagram of an implantable stimulator/sensor containing an oscillator to monitor the electrodes and lead failures as well as the living tissue state.

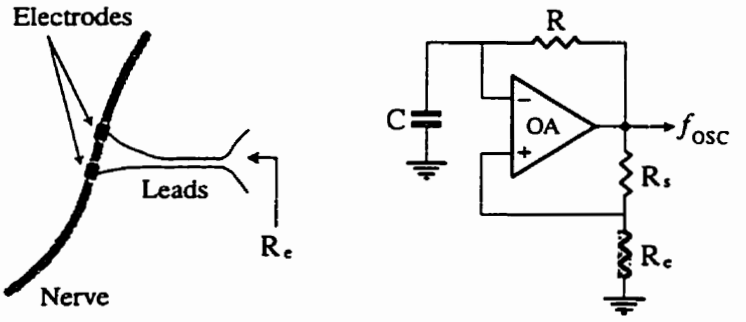


Fig. 4: Schematic diagram of the free-running oscillator employed to test a bipolar electrode and wire lead functionality.

3.2 Oscillator Design

The oscillator should be able to monitor fault in monopolar, bipolar, and tripolar electrodes. A grounded resistor should be therefore used to replace the electrode. Fig. 2 illustrates a single operational amplifier (OA) oscillator suitable for this purpose.

The OA and positive feedback resistors R_e and R_s form a Schmitt trigger. The signal to the OA's inverting input is provided by the circuit itself via the RC network. At low oscillation frequency the output voltage is a rectangular wave and the effect of the operational amplifier on the oscillation frequency can be neglected. At the oscillator start-up, V_O will be set either to $+V_{MAX}$ or to $-V_{MAX}$ which are only stable states allowed at the OA's output. With V_O equal to $+V_{MAX}$ the OA's positive input is set to $+V_T$ and the capacitor is charged exponentially toward V_{MAX} through resistor R until the OA's negative input reaches the $+V_T$ value which cause V_O to switch from $+V_{MAX}$ to $-V_{MAX}$. This also causes the OA's positive input snap to $-V_T$ and reverses the capacitor current so that the capacitor is now discharging toward $-V_{MAX}$ until the OA's negative input hits $-V_T$ which force V_O to snap to $+V_{MAX}$ and the same procedure is repeated.

As the capacitor is charged or discharged exponentially with a time constant RC, the time required for the OA's negative input to change from $-V_T$ to $+V_T$ is given by

$$t = RC \ln\left(\frac{V_{MAX} + V_T}{V_{MAX} - V_T}\right) \tag{1}$$

Considering that the duty cycle is 50 percent (f_{OSC} = ½ t) and by substituting $V_T = V_{MAX}\left(R_e/(R_e + R_s)\right)$ the oscillation frequency can be calculated from

$$f_{OSC} = \frac{1}{2RC \ln\left(1 + 2R_e/R_s\right)} \tag{2}$$

As the equation (2) implies, the oscillation frequency is not affected by the OA's output voltage level V_{MAX}. At high oscillation frequencies the slew-rate effect of OA must be considered.

A grounded resistance is able to represent both monopolar and bipolar electrodes. A tripolar electrodes may be considered as two bipolar electrodes with a common side and therefore should be tested in two steps. Hence, the electrode and tissue impedance replaces the component R_e in the oscillator. The percentage change in oscillation frequency for a given percentage change of R_e is called sensitivity of oscillation frequency to R_e and is defined as

$$S_{R_e}^{f_{osc}} = \frac{R_e}{f_{osc}} \frac{\partial f_{osc}}{\partial R_e} = \frac{-2R_e/R_s}{(1+2R_e/R_s)\ln(1+2R_e/R_s)} \tag{3}$$

This sensitivity is increased in magnitude when the ratio R_e/R_s is decreased. Therefore, to maximize the sensitivity of the oscillation frequency with respect to the leads and interelectrode impedance (R_e), the resistor R_s should be chosen much bigger than the nominal value of R_e.

3.3 Results

Main characteristics of the developed approach to monitor the bioelectronic interface of implantable devices are presented in this section. The oscillator has been designed using 1.2 μm CMOS technology and employs a two-stage CMOS operational amplifier to realize the OA block. The designed system has been laid out in Analog Artist environment of Cadence and the extracted layout has been extensively simulated using HSPICE simulator. The oscillator occupies a very small silicon area (0.045 mm^2) compared to a typical microstimulator implant (10 mm^2) [1] and can be implemented using very low-cost components. The layout of the oscillator is illustrated in Fig. 5.

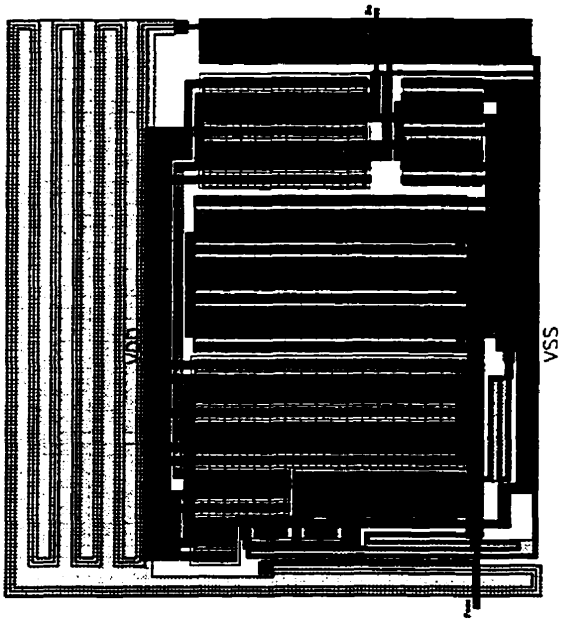


Fig. 5: Layout of the oscillator monitoring the electrode and leas failure.

Table 1 shows the oscillation frequency related to catastrophic faults in electrodes and leads. The variations of the oscillation frequency versus the parametric changes in the interelectrode impedance is illustrated in Fig. 6.

Table 1: Important values of the oscillation frequency.

R_e	f_{osc}
2 kΩ (normal condition)	55.3 kHz
100 Ω (a typical short circuit)	332 kHz
20 kΩ (a typical open circuit)	12 kHz

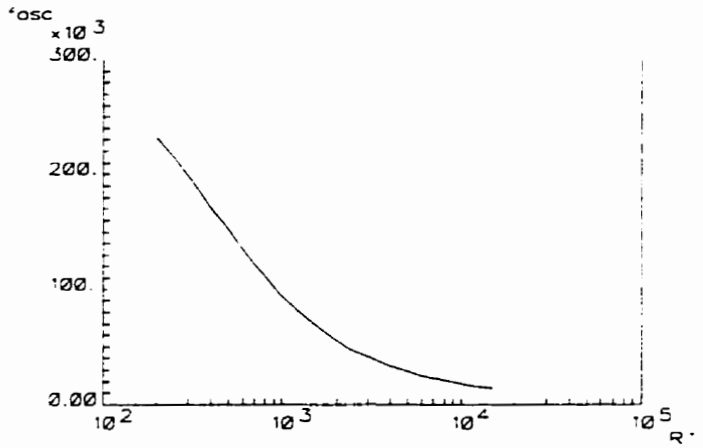
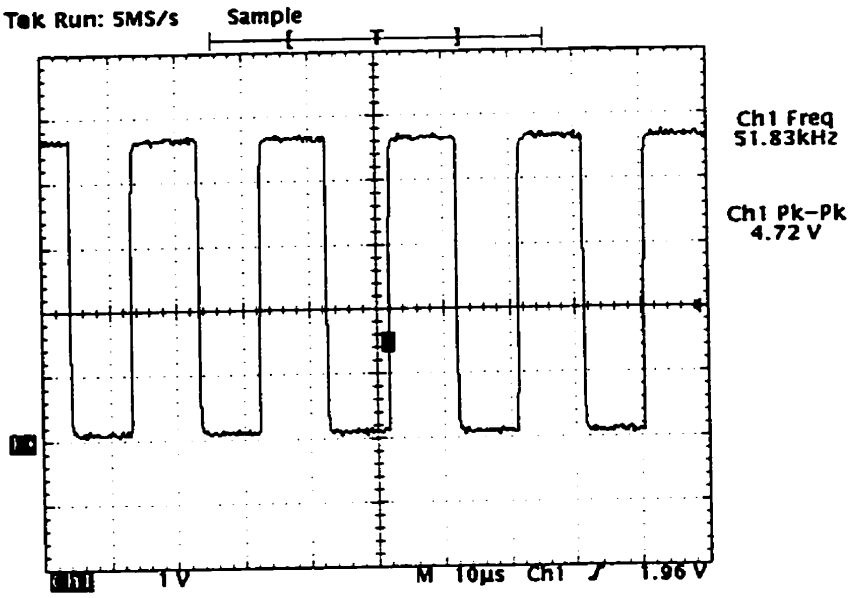
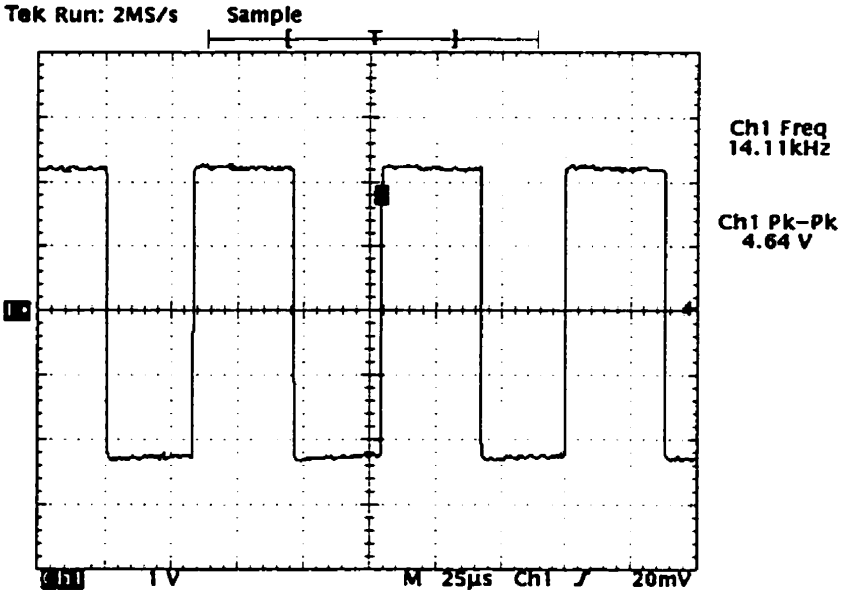


Fig. 6: Typical variations of the oscillation frequency versus the equivalent resistance of the interelectrode resistance.

The results show that both catastrophic (short and open circuits) and parametric variations are easily detectable. It should be noted that the oscillation frequency is a digital signal and can be evaluated using pure digital circuitry which is immune to noise.. The proposed test circuitry has been realized and tested using discrete components and typical monopolar bipolar cuff electrodes. Injected mechanical failures were fully detected during the in-vitro test and the results confirm the validity of the introduced approach. Fig. 7(a) illustrates a typical output signal of the oscillator in the monitoring phase when there is no fault in the electrode and wire leads. The output signal of the oscillator when one of wire leads is broken is shown in Fig. 7(b). In this experimentation, the oscillation frequency without fault is about 52 kHz and a breakage in wire leads deviates the oscillation frequency to 14 kHz. These results were captured by a digital Tektronic oscilloscope during the in-vitro test.



(a)



(b)

Fig. 7: The output signal of the oscillator without fault (a) and in the presence of a breakage in a wire lead (b).

4 Dedicated Monitoring Approach

Monitoring techniques can be more efficient or provide new features when dedicated to a specific application mainly because the approach can be optimized for a limited problem. In this section, we propose two different monitoring techniques for leads and electrodes functionality each of them dedicated to a specific application. Therefore, we first give a brief description of the system and then introduce the proposed solutions.

4.1 Monitoring Microstimulators' Bioelectronic Interface

An implantable microstimulator is an electronic device implanted inside body that produce and apply electrical stimulus to nerve or muscle to recuperate a lost function in the related organ. Current constant stimulus is widely used because the injected charge during stimulation can be more precisely controlled. Accurate control on the amount of charge injected is necessary to achieve a natural stimulation and to prevent charge accumulation which can destroy the nerve or muscle in chronic and continuos stimulations. Fig. 8 illustrates the block diagram of a stimulation channel of an implantable microstimulator. It is composed of a programmable digital stimulus generator (DSG), a 6-bit current mode digital-to-analog converter (DAC) and switching circuitry (SC). The SC directs the direction of current in the nerve or muscle and provides biphasic stimulation from a single positive supply voltage. The structure of this SC has been previously proposed in [14] and contributes a significant advancement in the design of output stage of implantable microstimulators.

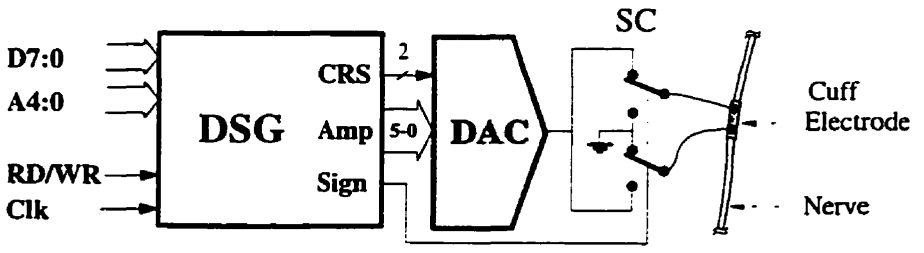


Fig. 8: Block diagram of a programmable stimulation channel (DSG: digital stimulus generator, RS: register selector, CRS: current range selector, and SC: switching circuitry).

Fig. 9 depicts a possible realization of the output stage. In fact, by taking into account the sign bit, it can be considered as a 7-bit current mode DAC devoted to electrical stimulation. V_{IN} is the voltage reference of the DAC which can be programmed to four different values using a flag register which is equivalent to 2-bits of more resolution.

The main design goal for this kind of application is to achieve low power consumption, a minimal silicon area, and an output with high linearity. In this example, the problem of matching positive and negative currents has been overcome, because the architecture of the DAC is based on single power supply (V_{DD}) and single voltage reference (V_{IN}) and therefore, sink and source currents are exactly matched. This matching is required to insure net charge balancing at the electrode site, conserving the reversibility of electrochemical reactions.

Six independent binary weighted current sources have been realized. Each of them is controlled by its equivalent bit coming from the control part of the microstimulator. The outputs of all current sources are connected together to obtain the sum of the currents directly in the nerve or muscle and therefor extra transistors which are conventionally used

to produce the sum of currents and mirroring it to the living tissue are eliminated. The *Sign* signal controls the direction of the current (I_{DAC}) in the nerve or muscle (R_e) to generate biphasic stimulation using a single power supply.

It should be noted that the current level of stimulus is determined by the DAC that generate a positive current. The direction of this positive current in the muscle or nerve is controlled using the *Sign* using the SC which produce both anodal and cathodal stimulations.

The voltage V_{Re} at the DAC's output equals $I_{DAC}R_e$ and can be used for our monitoring purpose. V_{Re} can be sampled and hold in both cathode and anode phase of stimulation and be converted to a frequency using a voltage-controlled oscillator (VCO).

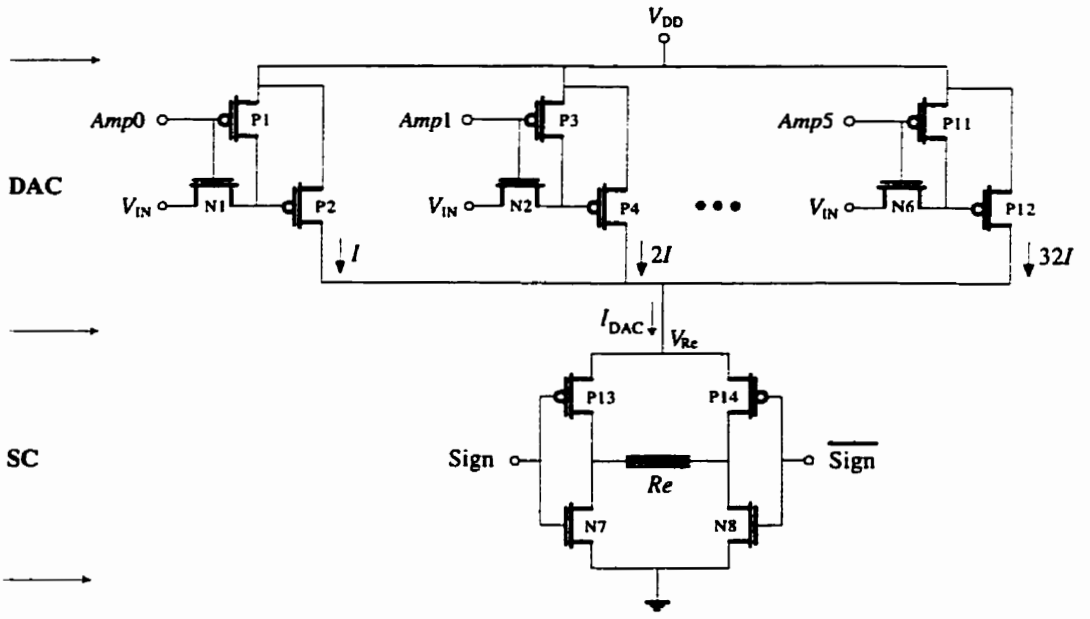


Fig. 9: Schematic view of a 6-bit bipolar current mode bipolar DAC (SC: switching circuitry).

Knowing I_{DAC} and measuring the oscillation frequency f_{OSC} the leads and interelectrode resistance R_e can be therefore deducted. As explained in section 2, by measuring this resistor we can localize fault in the bioelectronic interface of the microstimulator and evaluate the state of interelectrode tissue.

Fig. 10 represents, a simplified schematic of the stimulation channel's output stage with the necessary test circuitry to monitor fault in leads and electrode. The main advantage of this technique is that it can monitor the state of the bioelectronic interface without interrupting the stimulation process. This on-line monitoring capability is of great interest for the applications such as pacemakers that require continuos electrical stimulation. In this case the monitoring can be performed periodically without interrupting the stimulation.

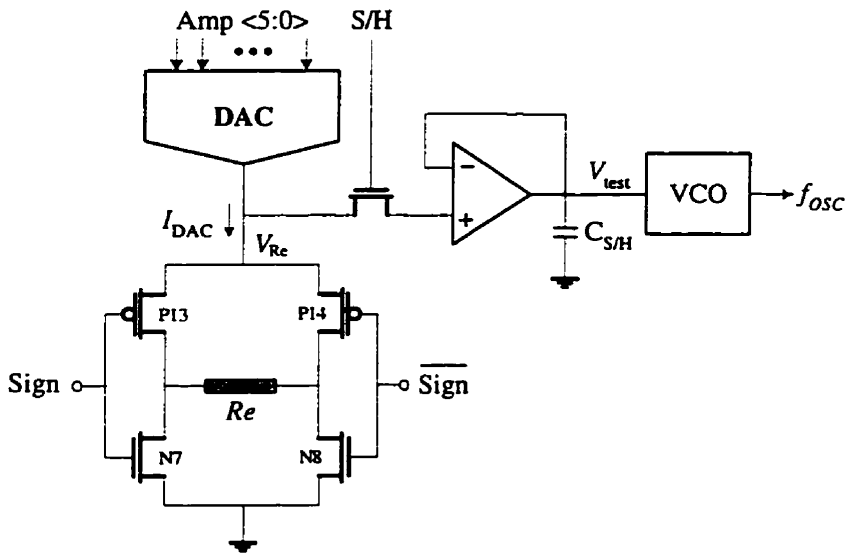
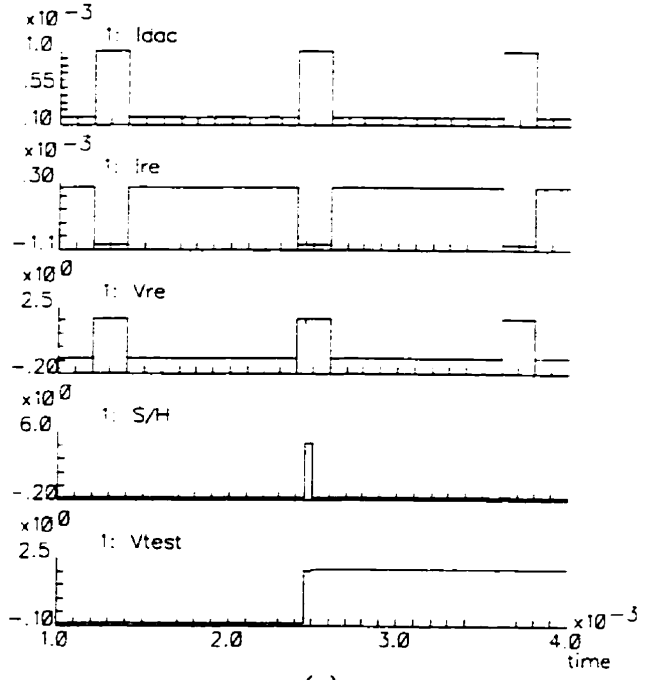


Fig. 10: Typical schematic of an implantable microstimulator including test circuitry.

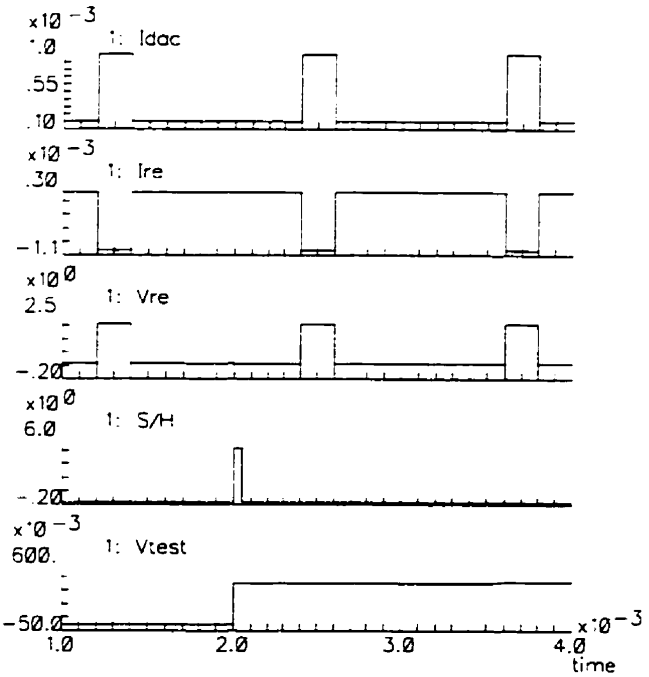
The operational amplifier has been used in unity-gain follower configuration to prevent the voltage sampling circuitry to affect the stimulation current during stimulation. Besides, the SC would not influence the accuracy of the voltage sampled V_{test}. V_{test} can be maintained precisely as long as the evaluation is required in the presence of the SC activity. Fig. 11 illustrates a typical biphasic stimulation generation and electrode monitoring in both cathode and anode stimulation phases.

It should be noted that the voltage V_{Re} is always positive because the current I_{DAC} is positive in both anode and cathode phases of stimulation. The first graph of Fig. 11(a) illustrates the current supplied by the DAC and the second graph shows the biphasic current passing through the living tissue. The third graph represents the output voltage of the DAC and the signal applied to the sample and hold circuit, S/H, is shown in the fourth graph. The last graph depicts the voltage $V_{test} = I_{Re} \times Re$ which is converted to a frequency using the voltage-controlled oscillator. As the current I_{Re} is known, the value of the equivalent resistance *Re* can be estimated from the resulting oscillation frequency.

A sample of in-vitro experimentation captured by a digital oscilloscope is presented in Fig. 12. The oscillation frequency was recorded just after the stimulation and after a long period of excessive stimulation and irritating the tissue by mechanical manipulations. The stimulus was a 100 Hz monophacic stimulation with 2 mA of current amplitude and 5 ms of pulse duration. The oscillator was designed to produce an oscillation frequency of 45 kHz in the normal condition. The result presented in Fig. 12 illustrate that this oscillation frequency drops to 36.5 kHz as a result of excessive stimulation and mechanical manipulation which increase the impedance of the interelectrode tissue.



(a)



(b)

Fig. 11: Biphasic stimulus generation and bioelectronic interface monitoring during the cathode phase (a) and the anode phase (b)of stimulation.

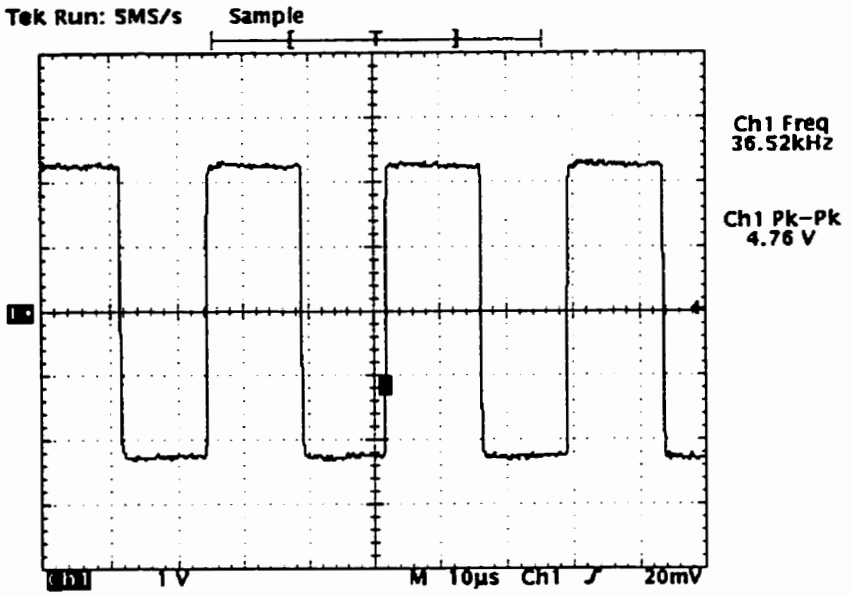


Fig. 12: The output signal of the oscillator after a long period of excessive stimulation.

4.2 Monitoring Sensors' Bioelectronic Interface

In general, biological signals are very small in amplitude and should be amplified before being processed. Instrumentation amplifiers which have a differential input, a very high differential gain, a high input impedance, a high common mode rejection ratio (CMRR), and low noise are frequently used as a preamplifier for bioelectric events. The use of operational amplifiers (op-amps) as active elements is an attractive way to construct a relatively simple instrumentation amplifier. The most popular architecture to construct an instrumentation amplifier is based on three op-amps as shown in Fig. 13. The recording of bioelectric events requires a very high overall gain which saturate the amplifier because of the presence of noise and the amplifier's input offset voltage. The accepted solution is to use the instrumentation amplifier with moderate gain (around 30 dB) as the first stage of

amplification, followed by several AC-coupled amplifier stage to obtain the required high overall gain. Furthermore, the three op-amp instrumentation amplifier can be chopper stabilized to minimize the effect of its offset voltage and equivalent noise at the output. The implementation of chopper stabilization technique in a three op-amp instrumentation amplifier is illustrated in Fig. 13. Multipliers which are controlled by a chopping square wave are inserted at the input and the output of the first stage of the instrumentation amplifier. The multipliers are implemented using two cross-coupled switches which are controlled by two nonoverlapping clocks ($\varphi 1$ and $\varphi 2$). After the first multiplier, the signal sensed is modulated and transferred to the odd harmonic frequencies of the chopping signal while the undesired signal consisting the instrumentation amplifier's input equivalent noise and offset voltage remains unaffected. After the second multiplier, the modulated signal is demodulated back to its original frequency but the undesired signal is now modulated to the odd harmonic frequencies of the chopping signal. Therefore, at the amplifier's output the undesired signal spectrum has been shifted to the odd harmonic frequencies of the chopping signal and the spectrum of signal sensed remains unaffected. Hence, the undesired signal can be filtered at the amplifier's output using a low-pass filter without affecting the original signal sensed by the electrode.

The voltage gain of this instrumentation amplifier is given by

$$\frac{V_o}{V_p - V_n} = \left(1 + \frac{2}{a}\right)\left(\frac{R1}{R2}\right) \tag{4}$$

The gain of this instrumentation amplifier is controlled by the factor a and the ratio of resistors R1 and R2. These resistors are chosen equal to provide unity-gain for the second stage of the amplifier. As the equation (4) demonstrates, disconnecting the resistor aR sets the gain of the first stage of the instrumentation amplifier to one.

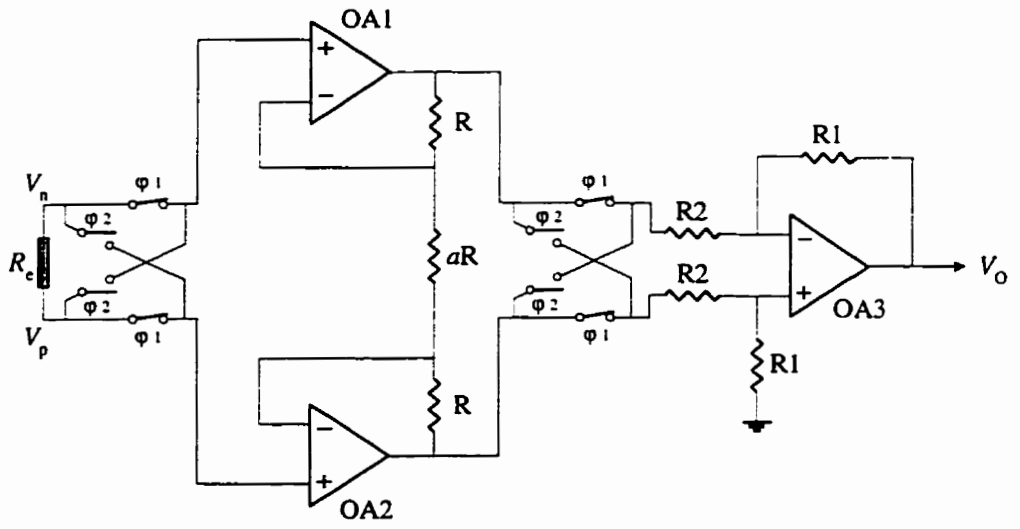


Fig. 13: Three op-amp instrumentation amplifier with chopping stabilization.

To monitor the bioelectronic interface in a sensor, we propose to reuse the monitoring facilities already available in the sensor's electronic circuitry. Fig. 14 depicts the instrumentation amplifier with the test circuitry providing the capability of monitoring the leads and electrode failure.

In the test mode, the signal S becomes active which cause a test current I_{TEST} to pass through the living tissue via the leads and electrode modeled by the resistor R_e. The first multiplier of chopper stabilization is working as in the normal mode and therefore the current I_{TEST} injected in the living tissue will be biphasic which prevent the electrode and tissue damage. At the same time, the activation of the signal S disconnects the resistor aR which modifies the overall gain of the instrumentation amplifier to unity. This prevents the saturation of the amplifier in the test mode because its input voltage in the test mode is relatively large. The second multiplier is not driven by signals φ1 and φ2 and the output of first amplification stage is directly passed to the second stage. Hence, the output

voltage V_O will be a constant DC voltage equal to $I_{TEST}R_e$ which can be used to measure the R_e value. It should be noted that as the output voltage V_O is constant the sample and hold circuitry is not required and it can be directly applied to a VCO for measurement.

A simulation result of the instrumentation amplifier in the test mode is illustrated in Fig. 15. The test current I_{TEST} is equal to 1 mA and the chopping signal is operating at 100 k Hz.

The instrumentation amplifier with monitoring facilities have been also realized using μA 741 op-amp and discrete elements. Available CMOS analog switches, DGP201A from *Siliconix Inc* have been employed to implement the test switches as well as the multipliers.

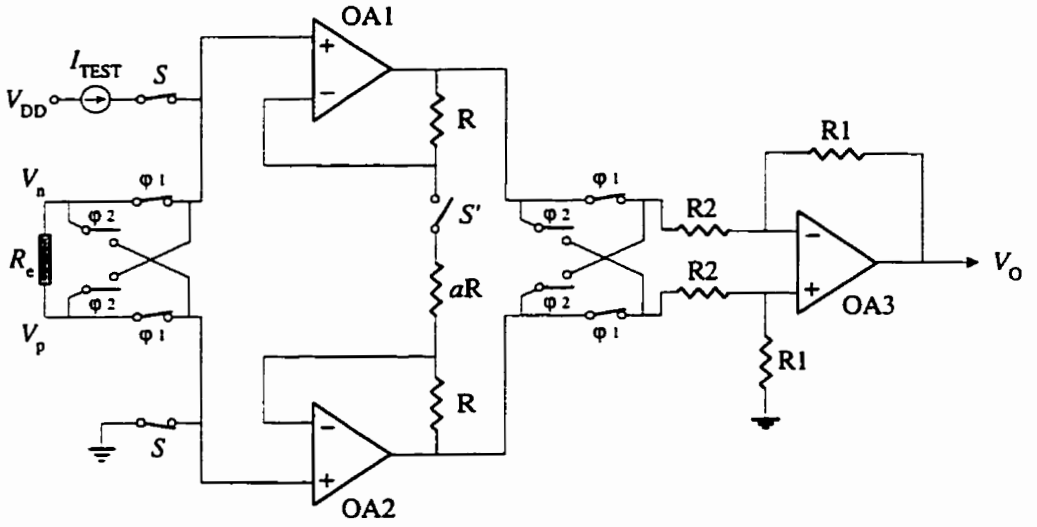


Fig. 14: Instrumentation amplifier with the ability of monitoring the bioelectronic interface of the implanted sensor.

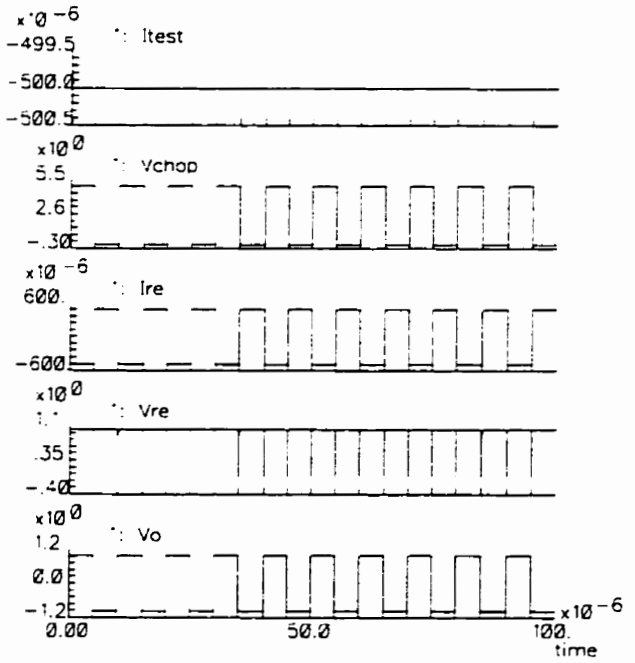


Fig. 15: Simulation of the three op-amp instrumentation amplifier in the test mode.

The practical results agree with the simulation results. The output voltage contains small glitches due to the switching activity of the first multiplier which are canceled by the low-pass filter which normally follows the instrumentation amplifier.

5 Conclusion

New techniques to test the functionality of implanted electrodes and leads, which increase the reliability of implanted microstimulators/sensors, have been introduced. The test technique is able to detect the failure type by evaluating the oscillation frequency. The same technique is used to monitor the state change and the fibrosis of the tissue in the vicinity of the electrode to help physician to compensate for them. The proposed approaches can be constructed using simple and low-cost components. The oscillator is

disconnected from the electrode and set in idle mode when no measurement is performed to minimize the power consumption. The feasibility of the introduced monitoring techniques has been demonstrated through extensive post-layout simulations and in-vitro experimentation.

References

[1] Arabi, K., and M. Sawan, "Implantable Multiporogrammable Microstimulator Dedicated to Bladder Control," Journal of *Med. & Biol. Eng. & Comput.*, 1995, vol. 34, pp. 9-12.

[2] Smith, B., P.H. Peckham, and W.K. Michael, "An Externally Powered, Multichannel, Implantable Stimulator for Versatile Control of Paralyzed Muscle," *IEEE Trans. on Biomed. Eng*, 1987, vol. 34, No. 7, pp. 499-507.

[3] Loeb, G.E., *et al.*, "An Injectable Microstimulator for Functional Electrical Stimulation," Journal of *Med. & Biol. Eng. & Comput.*, 1991, vol. 29, pp. NS13-NS19.

[4] Smith, S., and R. Aasen, "The Effects of Electromagnetic Fields on Cardiac Pacemakers," *IEEE Trans. on Broadcasting.*, Vol. 38, No. 2, 1992, pp. 136-139.

[5] Steyaert, M., and W. Sansen, "Low Power Monolithic Signal Conditioning System," *IEEE J. of Solid-State Circuits*, 1990, vol. 25, No. 2, pp. 609-612.

[6] Sansen, W., "On the Integration of an Internal Human Conditioning System," *IEEE J. of Solid-State Circuits*, 1982, Vol. SC-17, No. 3, pp. 513-521.

[7] Stotts, L.J., K.R. Infinger, J. Babka, and D. Genzer, "An 8-bit Microcomputer with Analog Subsystems for Implantable Biomedical Application," *IEEE J. of Solid-State Circuits*, 1989, Vol. 24, No. 2, pp. 292-299.

[8] Fernald, K.W., T.A. Cook, T.K. Miller, and J.J.Paulos, "A Microprocessor-Based Implantable Telemetry System," *IEEE Computer Mag.*, 1991, pp. 23-30

[9] Ji, J., and K.D. Wise, "An Implantable CMOS Circuit Interface for Multiplexed Microelectrode Recording Arrays," *IEEE J. of Solid-State Circuits*, 1992, Vol. 27, No. 3, pp. 433-443.

[10] Arabi, K., and B. Kaminska, "Parametric and Catastrophic Fault Coverage of Analog Circuits Using Oscillation-Test Methodology," Proc. of the *IEEE VLSI Test Symp.*, Monterey, April 1997, pp. 166-171.

[11] Dymond, A.M., "Characteristics of the Metal-Tissue Interface of Stimulation Electrodes," *IEEE Trans. on Biomed. Eng*, 1976, vol. BME-23, No. 4, pp. 274-280.

[12] Cobbold, R.S.C., "Transducers for Biomedical Measurements: Principles and Applications," *John Wiley & Sons*, Inc., New-York, Chap. 9 &10.

[13] Bey, P.P., *et al.* "Autonulling MOS Bridge for Sensor Applications," Proc. of the *IEEE EMBS Conf.*, 1991, pp. 1595-1596.

[14] Arabi, K., "Conception d'un microstimulateur neuromusculaire implantable destiné à la récupération de dysfonctions urinaires," *M.Sc. Thesis*, École Polytechnique de Montréal, July 1994, 180 p.

CHAPITRE 5

CAPTEURS DE TEMPÉRATURE INTÉGRÉS POUR LA VÉRIFICATION DE L'ÉTAT THERMIQUE DES PUCES DÉDIÉES

5.1 Résumé

Le nombre de transistors pouvant être intégrés dans un circuit VLSI peut atteindre plusieurs millions. De plus, la fréquence d'opération des circuits électroniques dans une technologie CMOS peut dépasser quelques cents MHz. Le nombre de transistors et la vitesse de fonctionnement d'un circuit intégré sont parmi les facteurs essentiels qui déterminent sa dissipation de puissance. C'est pourquoi que la consommation de l'énergie est devenue un paramètre critique même pour les circuits CMOS.

La consommation de puissance excessive dans une région d'un circuit intégré augment la température de la région et provoque des pannes physiques causant le mauvais fonctionnement du circuit intégré. En outre, la consommation d'énergie est un facteur critique pour les circuits implantables et doit être sévèrement surveillée.

5.2 "Built-In Temperature Sensors for On-line Thermal Monitoring of Microelectronic Structures"

Du point de vue de la fiabilité le monitoring de l'état thermique des structures microélectronique est très important. Il permet de prévenir l'occurrence éventuelle des

pannes dues aux températures excessive de la puce dédiée et d'estimer la durée de vie de la pile implantée.

Dans ce chapitre, nous proposons d'utiliser des capteurs de températures intégrés pour vérifier l'état thermique de la puce dédiée. Les capteurs sont insérés dans les régions critiques de la puce. Une température élevée indique la possibilité éventuelle d'avoir des pannes dans le circuit intégré. L'article présentée dans ce chapitre est accepté pour publication dans le *Journal of Electronic Testing: Theory and Applications* (*JETTA*) de *Kluwer Academic Publishers.*

Built-In Temperature Sensors for On-line Thermal Monitoring of Microelectronic Structures

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Abstract

Built-in temperature sensors increase the system reliability by predicting eventual faults caused by excessive chip temperatures. In this paper, simple and efficient built-in temperature sensors for the on-line thermal monitoring of microelectronic structures are introduced. The proposed temperature sensors produce a signal oscillating at a frequency proportional to the temperature of the microelectronic structure and therefore they are compatible to the oscillation-test method. The oscillation-test method is a low-cost and robust test method for mixed-signal integrated circuits based on transforming the circuit under test (CUT) to an oscillator. This paper presents the design and detailed characteristics of the sensors proposed based on a CMOS 1.2 μm technology parameters. The fabrication results show a small spread in the nominal oscillation frequency of sensors

implemeted and a good sensitivity of the oscillation frequency with respect to temperature variations. The sensors proposed require very small power dissipation and silicon area.

Key Words: Temperature sensor, Thermal monitoring, On-line testing, BIST, Oscillation-test strategy.

1 Introduction

Due to the advances in the fabrication process of integrated circuits and the market requirements, the trend of designing complex mixed-signal application specific integrated circuits (ASICs) has been increased. By enlarging an integrated circuit, its power dissipation increases and the temperature of the microelectronic structure increases. This problem is especially magnified in circuits operating at high frequencies. Besides, some short circuit faults, which may not necessarily be a functional fault, increase the power dissipation and consequently increase the chip temperature. Therefore, the thermal state of integrated circuits has been always a problem of great concern and is considered as a bottle-neck in increasing the integration of electronic systems.

To overcome this problem many researchers are developing low-power design techniques for VLSI systems [1],[2]. From the reliability and test point of view, life-time, continuous thermal verification would be useful to detect excessive power dissipation, which eventually causes chip deterioration. In this paper, we present new temperature sensors for thermal monitoring of microelectronics structures suitable for built-in self-test (BIST) of integrated circuits using the oscillation-test strategy. The paper is organized as follows. Section 2 introduces an overview of the oscillation-test method. The basic principles of thermal sensors is briefly reviewed in section 3. The design and specifications of the proposed temperature sensors are presented in section 4.

2 Oscillation-Test Strategy (OTS)

This test method is based on partitioning a complex analog circuit into functional building blocks, such as amplifier, operational amplifier (OA), comparator, Schmitt trigger, filter, voltage reference, oscillator, phase lock loop (PLL), etc., or a combination of these blocks [3]-[5]. During the test mode, each building block is converted to a circuit which oscillates. The oscillation frequency f_{osc} of each building block can be expressed as a function of either its components or its important parameters. The building blocks which inherently generate a frequency, such as oscillators, do not need to be rearranged, and their output frequency is directly evaluated.

The observability of a faulty component (or parameter) is defined as the sensitivity of the oscillation frequency f_{osc} with respect to the variations of the component (or the parameter). A fault is said to be detectable if it causes a reasonable deviation of the oscillation frequency from its tolerance band. The tolerance band of f_{osc} for each CUT is determined based on a Monte Carlo analysis of the converted CUT taking into account the nominal tolerance of all important technology and design parameters. Faults in the CUT related to components (or parameters) which are involved in the oscillator structure manifest themselves as a deviation of the oscillation frequency. Therefore, the deviation of the oscillation frequency from its nominal value may be employed to detect a fault.

A global block diagram of the oscillation built-in self-test (OBIST) technique based on oscillation-test strategy is illustrated in Fig. 1. The OBIST circuitry is composed of an analog multiplexer (AMUX) to direct the CUT test points to the BIST circuitry, a frequency-to-number converter (FNC) which converts the oscillation frequency selected by AMUX to an M-bit number, and control logic (CL) which directs all operations and produces the pass or fail test result.

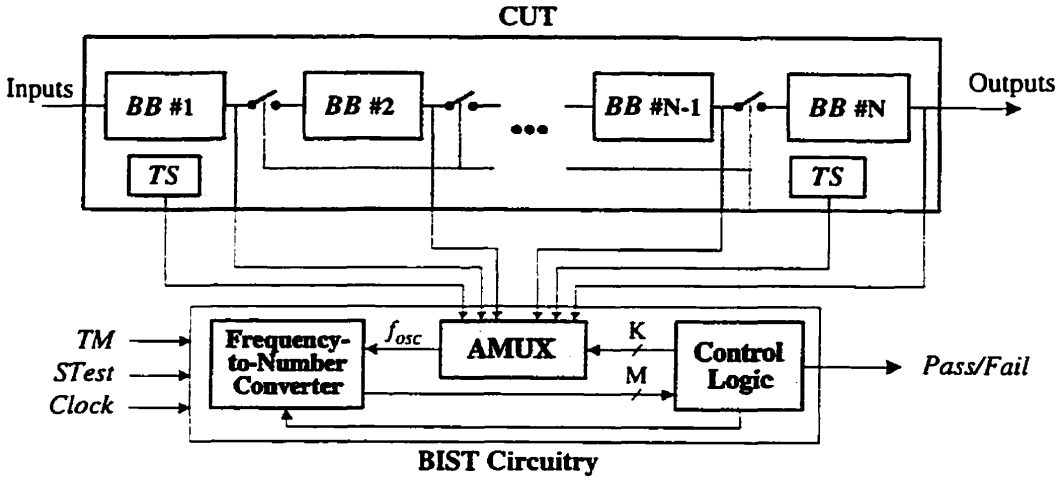


Fig. 1: Global plain view of the oscillation built-in self-test (OBIST) structure proposed for the oscillation-test methodology (*BB*: building block, *TS*: temperature sensor, *TM*: test mode, *STest*: self-test mode, AMUX: analog multiplexer).

In this paper, the OBIST structure is supported with some temperature-controlled oscillators used as sensors to monitor the thermal state of the chip under test. These sensors are implemented at some critical points on the chip and produce a frequency related to the temperature sensed.

The analog multiplexer (AMUX) selects the test point extracted from the converted building block. The oscillation frequency of the selected test point is then converted to a number using the frequency-to-number converter, and is evaluated by the control logic. To verify the functionality of the test structure, the test circuitry is tested during the self-test phase before the CUT is tested. Following sections presents the detailed characteristics of the chip temperature sensors.

3 Electronic Temperature Sensing

Temperature measurement has widespread applications from industrial control to medical diagnosis. One of the most common ways of temperature sensing is to use electronic sensors. The advantage of electronic temperature sensing using integrated circuit (IC) sensors is that signal conditioning can be performed on the same chip, so that no other component is required and the sensor output can be directly used by another electronic system. Furthermore, well matched elements can be realized within the same chip which eliminates the source of many errors. Electronic temperature sensors are classified under three main categories: thermocouples, active devices such as diodes and transistors and thermoresistors.

3.1 Thermocouples

A thermocouple is constructed using two junctions of different metals held at different temperatures. Although thermocouples can be integrated using Seebeck effect of silicon, they require a big chip surface [7]. Another problem is the inability of thermocouples to measure the absolute temperature values which implies the need for a reference temperature. Due to silicon's high thermal conductivity, a chip is nearly isothermal and it would be difficult to separate the reference temperature and the thermocouple sensor.

3.2 Active Devices

Silicon diodes and bipolar transistors are regularly used for temperature sensing [9]. In diode based sensors, the *pn* junction is forward biased by a constant current, with the forward voltage measured as a means of temperature sensing. Diodes can be used for accurate temperature measurements only after careful calibration. A bipolar's base-

emitter voltage-temperature characteristics for a constant collector current has the same form as the diode forward voltage curve. Diode's forward voltage and the base-emitter voltage (V_{BE}) of a bipolar transistor have negative temperature coefficient. The difference ΔV_{BE} between the values of V_{BE} of two identical transistors, except for size, when operated at different current densities, depends only on the thermal voltage ($V_T = kT/q$) and the ratio of the current densities. ΔV_{BE} is proportional to the absolute temperature (PTAT). ΔV_{BE} is a very small voltage and therefore susceptible to noise and nonideal factors in V_{BE}. In any standard CMOS technology, two types of parasitic bipolar transistors can be realized: a vertical and a lateral bipolar transistor. These parasitic transistors can be employed to realize bipolar transistor-based temperature sensors in CMOS technologies. Weak-inversion MOS transistors also exhibit a diode-like exponential current-voltage relationship which has been used to construct temperature sensors. It should be noted that the effects of leakage currents start to become significant in MOS transistors operated in weak inversion region at temperatures below 60°C, so that they are impractical for a wide range of temperatures [10].

3.3 Thermoresistors

The electrical resistivity of both metals and semiconductors varies with temperature and has been used to monitor the temperature. Comparing to semiconductors, metals represent a better linearity over a large range of temperature but their small absolute resistance value makes them non-suitable for integrated sensors. The main advantage of semiconductors as temperature sensor is that they can be distributed over a given surface and therefore the resistance change will be proportional to average temperature of that region. In the other words, semiconductor resistors measure the average temperature of a given area rather than the temperature of a point of the integrated circuitwazzu . The *n*-

well, *p*-well and polysilicon resistors are widely used as temperature sensor elements in MOS and bipolar technologies. The well resistors shows a higher sensitivity to temperature than the polysilicon resistors. However, the resistance of heavily doped polysilicon resistor increases more linearly with temperature [11].

4 On-line Built-In Thermal Testing

As it can be concluded from the previous section, there are various temperature sensors suitable for thermal state verification of integrated circuit microstructures, such as thermoresistors, *pn* junctions and the exploitation of the weak-inversion of MOS transistors. Our objective is to convert the temperature sensed to an oscillating signal in order to make it compatible to the oscillation-test method and facilitate the evaluation of the temperature sensed. A temperature sensor based on a ring-oscillator has been already introduced in [6]. This cell guarantees a 3°C accuracy that is marginally acceptable as a chip temperature sensor but the silicon area required by the sensor is rather big. The principle of the thermally-feedbacked oscillator has been also introduced in [7]. Recently a MOS temperature-controlled oscillator was used as a sensor to monitor the thermal state of microelectronic structures [8] in which the frequency-determining feedback element is realized using a thermal time-delay line. The internal thermal diffusion constant of the silicon is reasonably sensitive to temperature variations and is therefore used for temperature sensing. However, it requires about 10 to 15 mW power to drive the thermal delay line and the dissipator transistor [8].

To overcome theses inconveniences, we present in this paper three new built-in temperature sensors having a very small power dissipation and silicon area. The *n*-well resistor has been chosen as the temperature dependent component because of its high temperature coefficient comparing to other integrated resistor realizations such as

diffusion and polysilicon resistors. The temperature coefficient of the *n*-well sheet resistor in the Mitel S.C.C. 1.2 μm technology is around 6100 ppm/°C.

Ring and relaxation oscillators are relatively simple and have stable and guaranteed oscillations. Therefore, the temperature sensitive component is incorporated in ring and relaxation oscillators to control the oscillation frequency. Three different types of temperature sensors based on the ring oscillator concept have been designed and evaluated using the Mitel 1.2 μm technology.

4.1 RC Delay Controlled Ring Oscillator-Based Temperature Sensor (DCRTS)

Fig. 2 illustrates a 3-stage ring oscillator which comprises additional RC delay elements. The layout of this temperature sensor shown in Fig. 3 occupies around 0.0174 mm^2 of silicon area. Variation of *R* and *C* components affect the loop delay and therefore changes the oscillation frequency. Due to the fact that the capacitors are not very sensitive to temperature variations and the inverters' delay is neglectable comparing to delay introduced by *R* and *C* components, the frequency of oscillation is dominantly controlled by the resistors as a result of temperature variations.

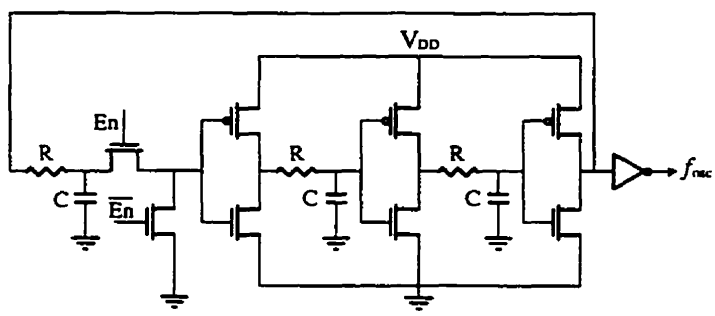


Fig. 2: Schematic diagram of the RC delay controlled temperature sensor.

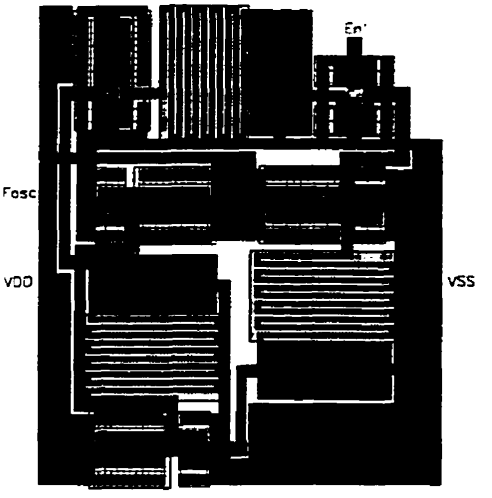


Fig. 3: Layout of the RC delay controlled ring oscillator employed as temperature sensor.

The oscillation period of the ring oscillator is equal to the sum of the delays introduced by inverters and therefore it can be estimated by

$$f_{osc} = 1/3(PD^{+} + PD^{-}) \tag{1}$$

where PD^{+} and PD^{-} represent the positive and negative propagation delays of each inverter and we supposed that the 3 inverters are similar.

The propagation delay for each stage is defined as the time it takes for its output voltage to make the transition from its quiescent state to the trip point V_{TRP} of the following stage. Using the square law model of a MOSFET [12], the trip voltage of an inverter can be calculated by the following equation

$$V_{TRP} = \frac{V_{DD} - |V_{tp}| + V_{tn}\sqrt{\beta_n/\beta_p}}{1 + \sqrt{\beta_n/\beta_p}} \tag{2}$$

where $\beta = (\mu C_{OX})\dfrac{W}{L}$ and V_{tn} and V_{tp} denote the threshold voltage of NMOS and PMOS transistors receptively. The parameter μ is the carrier mobility and C_{OX} is the gate capacity per unit area of a MOS transistor. The equation for V_{TRP} is derived from the

approximation that the output voltage of an inverter changes its state when the current in PMOS and NMOS transistors (in saturation) are equal.

Neglecting the on resistance and the parasitic capacitor of each inverter comparing to R and C, the positive and negative propagation delays can be calculated using the following relationships

$$PD^{+} = -RC\ln\left(1 - \frac{V_{TRP}}{V_{DD}}\right) \tag{3}$$

$$PD^{-} = -RC\ln\left(\frac{V_{TRP}}{V_{DD}}\right) \tag{4}$$

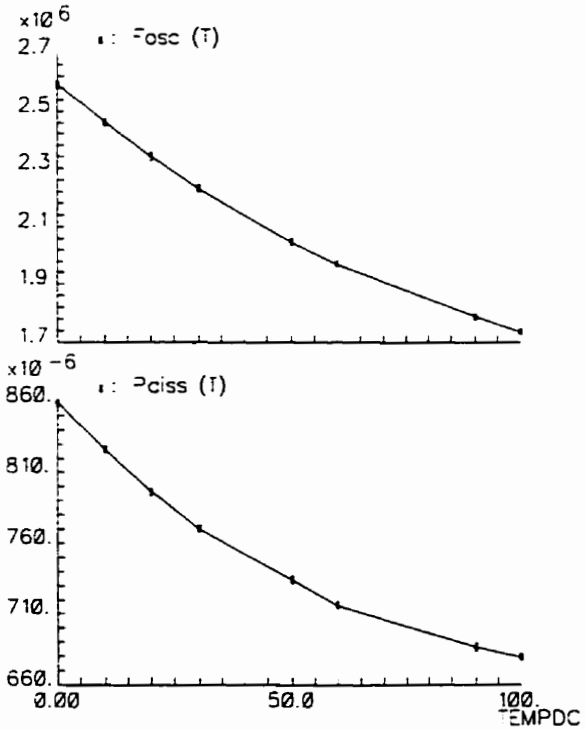


Fig. 4: Oscillation frequency and sensor power dissipation versus the chip temperature. The horizontal axis represents the chip temperature (TEMPDC).

Substituting PD^+ and PD^- in equation (1) the oscillation frequency is obtained as

$$f_{osc} = \frac{1}{3RC\ln\left(\frac{V_{DD}^2}{(V_{DD} - V_{TRP})V_{TRP}}\right)} \tag{5}$$

The upper graph of Fig. 4 depicts the variation of the oscillation frequency versus the chip temperature. The power dissipation of the temperature sensor as a function of the chip temperature is illustrated in the lower graph of Fig. 4. The maximum power dissipation of the sensor is 0.86 mW which happens at 0 °C. To prevent unnecessary power consumption, the temperature sensor is enabled using a control signal (*En*) only during testing periods. Fig. 5 presents the output voltage and supply current of the temperature sensor when the state of the *En* signal is changed.

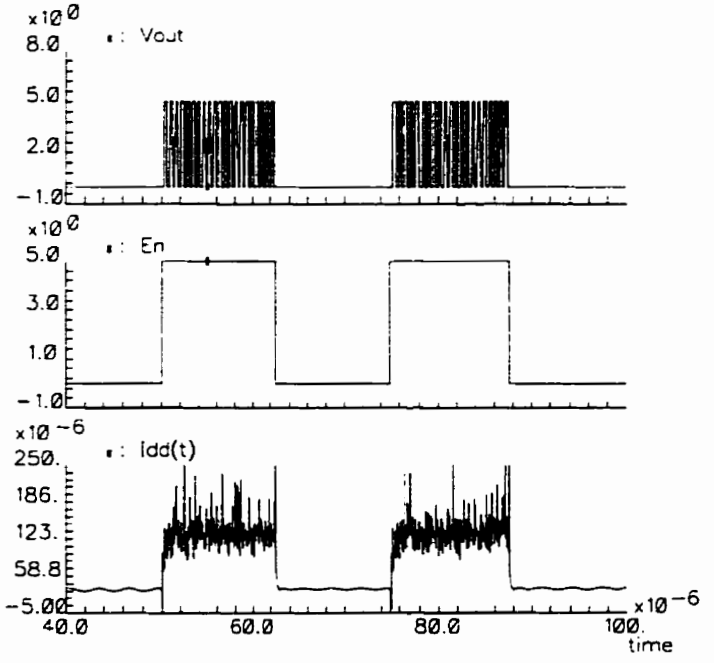


Fig. 5: *RC* delay-based temperature sensor output voltage and its current dissipation.

4.2 Current-Controlled Ring Oscillator Based Temperature Sensor (CCRTS)

The heart of the second temperature sensor is a current-controlled current-mode ring-oscillator shown in Fig. 6. The oscillator employs five stages of inverters instead of three stages to provide the same nominal oscillation frequency as the first temperature sensor and also to obtain a faster start-up and more stable oscillations due to increased closed-loop gain. The rise-time and fall-time of the oscillating signal is determined by the source and sink currents (I) available at the output of each current-mode inverter, the input capacitor of the next stage, and the threshold voltage of the inverters. Therefore, a suitable way to control the oscillation frequency is to change these currents. Post-layout simulations show that a wide range of oscillation frequencies having 50% duty cycle and low jitter can be produced using this oscillator.

The current controlling the oscillation frequency is provided using a temperature sensitive resistor and mirrored to drive all stages of the ring oscillator. When the temperature increases the resistor value increases and consequently the current controlling the oscillator decreases which results in a decrease in the oscillation frequency. Therefore, a temperature-controlled oscillator has been achieved. The propagation delay of each inverter is determined by its sink and source current I and the equivalent parasitic capacitor at the inverter output C_C. As the parasitic capacitor is charged or discharge using constant current I, therefore the positive and negative propagation delays of an inverter can be calculated using the following relationships

$$PD^{+} = \frac{C_C V_{TRP}}{I} \tag{6}$$

$$PD^{-} = \frac{C_C (V_{DD} - V_{TRP})}{I} \tag{7}$$

$$f_{OSC} = \frac{1}{5\left(PD^{+} + PD^{-}\right)} = \frac{I}{5C_C V_{DD}} \tag{8}$$

The reference current I is given by

$$I = \left(V_{DD} - V_{gsP1}\right)/R_S \tag{9}$$

Using the square law model of a MOSFET, the gate-source voltage of the transistor P1 is given by

$$V_{gsP1} = V_{tP1} + \sqrt{\frac{2IL_{P1}}{K' W_{P1}}} \tag{10}$$

As the current I is small and the W/L ratio of the transistor P1 is chosen to be big, the V_{gsP1} can be approximated to the threshold voltage of transistor P1 (V_{tP1}) and therefore the oscillation frequency is found to be

$$f_{OSC} = \left(\frac{V_{DD} - V_{tP1}}{V_{DD}}\right)\frac{1}{5R_S C_C} \tag{11}$$

The sensitivity of the oscillation frequency with respect to the power supply voltage variation can be derived as

$$S_{V_{DD}}^{f_{OSC}} = \frac{V_{DD}}{f_{OSC}}\frac{\partial f_{OSC}}{\partial V_{DD}} = \frac{V_{tP1}}{V_{DD} - V_{tP1}} \tag{12}$$

Substituting V_{DD}=5 V and V_{tP1}=0.9 V, the sensitivity is found to approximately equal to 0.22.

Layout of this temperature sensor is presented in Fig. 7 and occupies about 0.03 mm^2 of active silicon area.

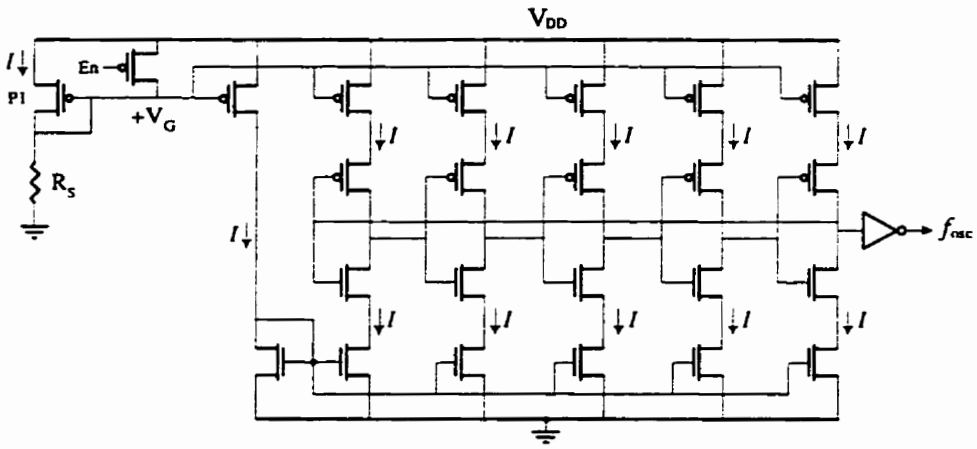


Fig. 6: Schematic diagram of the built-in temperature sensor. Currents I_1 and I_2 are chosen to be equal.

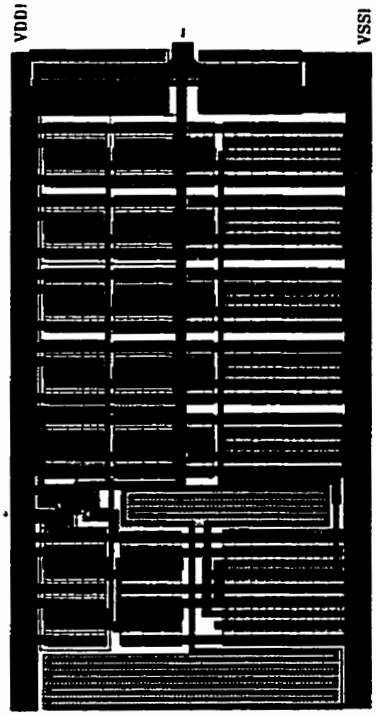


Fig. 7: Layout of the current-controlled temperature sensor.

The temperature coefficient of a given parameter P (TC) is defined using the differential sensitivity function as follows

$$TC_P = \frac{1}{T} S_T^P = \frac{1}{P} \frac{\partial P}{\partial T} \tag{13}$$

As the temperature coefficient of the capacitor is normally very small therefore the temperature dependency of the oscillation frequency is dominated by the temperature coefficient of the resistor R_S and that of P1 transistor threshold voltage V_{tP1}. Using the equation (11) the temperature coefficient of the oscillation frequency ($TC_{f_{OSC}}$) is given by

$$TC_{fosc} = -\left(\frac{1}{V_{DD} - V_{tP1}} \frac{\partial V_{tP1}}{\partial} + \frac{1}{R_S} \frac{\partial R_S}{\partial T} \right) \tag{14}$$

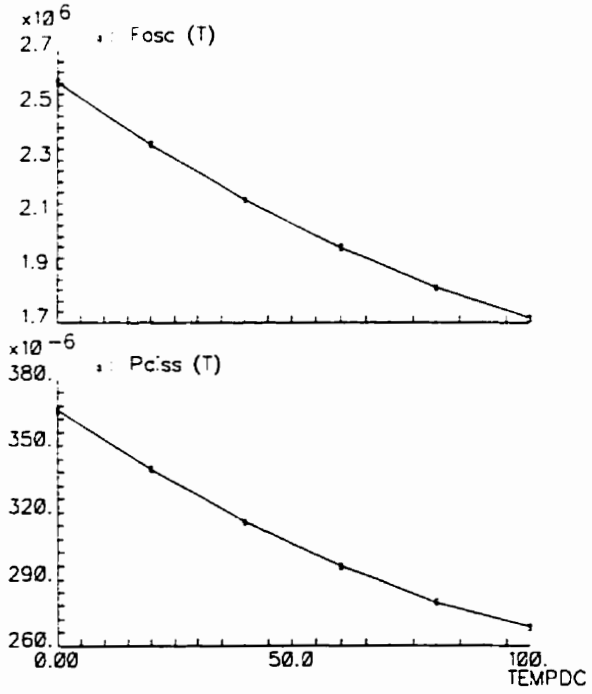


Fig. 8: Oscillation frequency and sensor's power dissipation versus the chip temperature. The horizontal axis represents the chip temperature (TEMPDC).

The upper part of Fig. 8 shows the variation of oscillation frequency versus chip temperature. The effective supply current of the sensor for different temperature values is given in the lower graph of Fig. 8. The maximum power dissipation (0.37 mW) occurs at 0 °C because at this temperature the oscillation frequency is maximum. Fig. 9 illustrates the sensor's output signal and its supply current along with the effect of *En* signal.

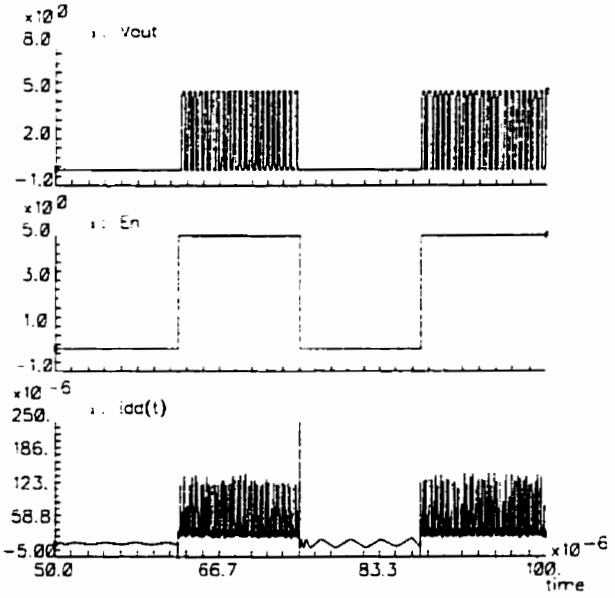


Fig. 9: Current-controlled temperature sensor's output voltage and its current dissipation.

4.3 Current-Controlled Relaxation Oscillator-Based Temperature Sensor (CCXTS)

An ideal temperature sensor should be sensitive to temperature but immune to other deviations such as power supply voltage variation. The common drawback of the fist two temperature sensors proposed in this paper is their susceptivity to supply voltage variations. In this section, we propose a temperature sensor which is less sensitive to supply voltage. The proposed sensor structure is based on a current controlled relaxation oscillator as shown in Fig. 10.

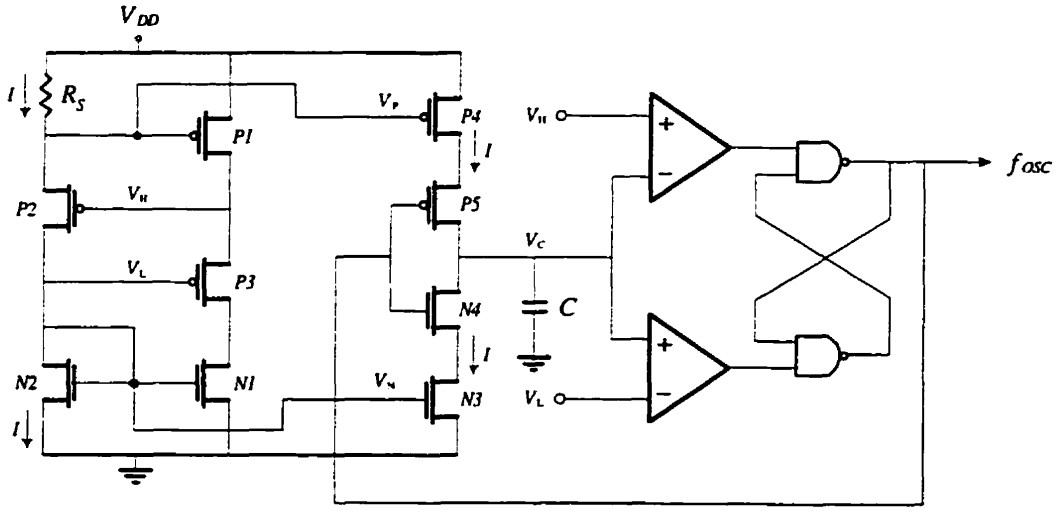


Fig. 10: Temperature sensor designed based on a current-controlled relaxation oscillator.

Similar to the approach proposed in the previous section, the sensitivity of a resistor to temperature is used to produce a temperature sensitive current which drives a current-controlled oscillator. The temperature-sensitive resistor is implemented in a current reference generator which also establishes the voltage references V_N, V_P, V_L, and V_H. The produced current I is mirrored using the transistors P4 and N3 to provide the same source and sink current to charge and discharge the capacitor C. It should be noted that as both source and sink currents stem from the same current source they have a similar temperature coefficient and are nominally equal to I. Assume initially that the f_{OSC} have the logic value 0 and therefore the transistor P5 is on and the transistor N4 is off causing the capacitor C to be charged using the source current I until V_C exceeds the upper threshold V_H. When this occurs the output latch toggles and the logic value of f_{OSC} becomes logic 1 which in turn make the transistor P5 off and the transistor N4 on. This forces the capacitor C to be discharged by the sink current I until the capacitor voltage falls below a lower threshold V_L at which time the entire cycle repeats. Neglecting the

delay introduced by comparators, latch and transistors P5 and N4, the oscillation frequency is given by

$$f_{osc} = \frac{I}{2C(V_H - V_L)} \tag{15}$$

As the current I is sensitive to temperature, therefore the oscillation frequency is directly proportional to temperature variations. The layout of the temperature sensor is presented in Fig. 11 which occupies 0.0565 mm^2 of silicon area.

Before estimating the temperature coefficient of this temperature sensor, we will briefly explain the basic principles of the voltage and current reference generator.

The main principle behind the reference generator is to use the voltage across the gate-source of an NMOS active device to create a current and then reproducing the original current passing through the active device using this current. this technique called V_t referenced source or bootstrap reference provides current and voltage references that are for all practical purposes independent of V_{DD} [12]. As shown in Fig. 10, the V_{gsP1} causes the current I to flow through R_S. The current I is mirrored using the transistors P2, P3, N1, and N2 and passed through the transistor P1 to recreate the voltage V_{gsP1}. Therefore, the current passing through the resistor R_S and the transistor P1 are equal.

The gate-source voltage of the transistor P1 in saturation region is given by

$$V_{gsP1} = V_{tP1} + \sqrt{\frac{2IL_{P1}}{K' W_{P1}}} \tag{16}$$

The voltage across the resistor R_S can be calculated using ohm's law

$$V_{R_S} = IR_S \tag{17}$$

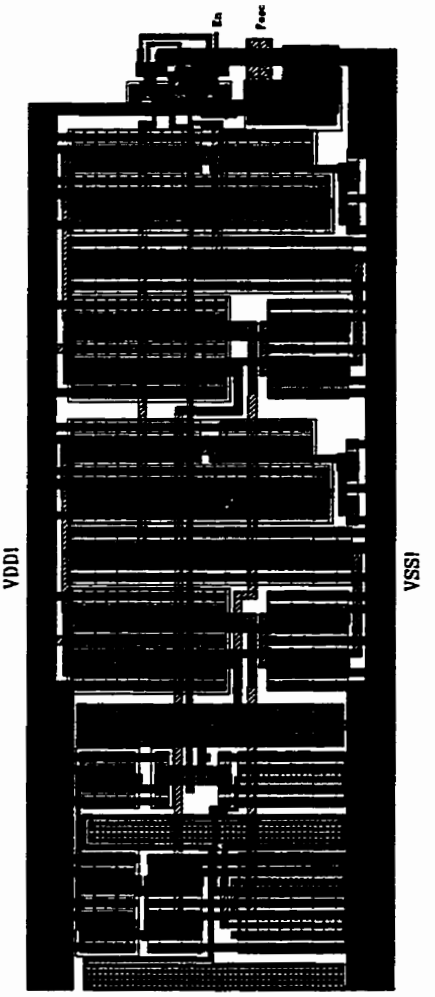


Fig. 11. Layout of the current-controlled relaxation oscillator-based temperature sensor.

As these tow voltages are connected together an equilibrium point is established which is described using the following equation

$$IR_S = V_{tP1} + \sqrt{\frac{2IL_{P1}}{K' W_{P1}}} \tag{18}$$

Providing that the W/L ratio of the transistor P1 is big enough and the current I is very small we can assume that V_{gsP1} is approximately equal to its threshold voltage V_{tP1} and therefore

$$I \approx \frac{V_{tP1}}{R_S} \tag{19}$$

This equation implies that the current I is not affected by V_{DD} and its sensitivity with respect to V_{DD} is essentially zero. Looking at the equation (15), one can find that the oscillation frequency depends also on the difference voltage (V_H- V_L) given by

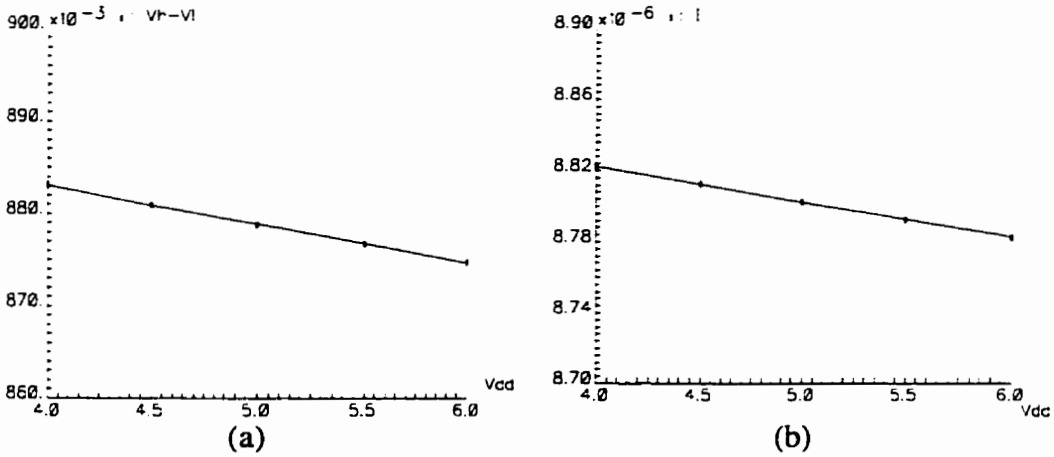
$$V_L = V_{DD} - V_{gsP1} - V_{gsP2} \tag{20}$$

$$V_H = V_{DD} - V_{gsP1} - V_{gsP2} - V_{gsP3} \tag{21}$$

$$V_H - V_L = V_{gsP3} \tag{22}$$

It should be noted that the W/L ratio of P1, P2, and P3 transistors is chosen big enough to be able to approximate their V_{gs} to V_t and therefore V_H-V_L = V_{tP3}. The oscillation frequency of the temperature sensor can be found as

$$f_{osc} = \frac{V_{tP1}}{2R_S C V_{tP3}} \approx \frac{1}{2R_S C} \tag{23}$$



(a) (b)

Fig. 12. Variation of current and voltage references versus power supply voltage changes.

The variation of current reference I and voltage references versus power supply voltage is illustrated in Fig. 12 and demonstrate that they are almost independent of changes in V_{DD} level.

Ignoring the temperature dependency of the capacitor C and using the equation (23) the temperature coefficient of the oscillation frequency ($TC_{f_{osc}}$) is given by

$$TC_{fosc} = -\frac{1}{R_S}\frac{\partial R_S}{\partial T} \tag{24}$$

The temperature dependency of voltage and current references are presented in Fig. 13. The variation of the relaxation oscillator-based sensor oscillation frequency and power dissipation versus the chip temperature is illustrated in Fig. 14. The maximum sensor power dissipation is around 0.490 mW.

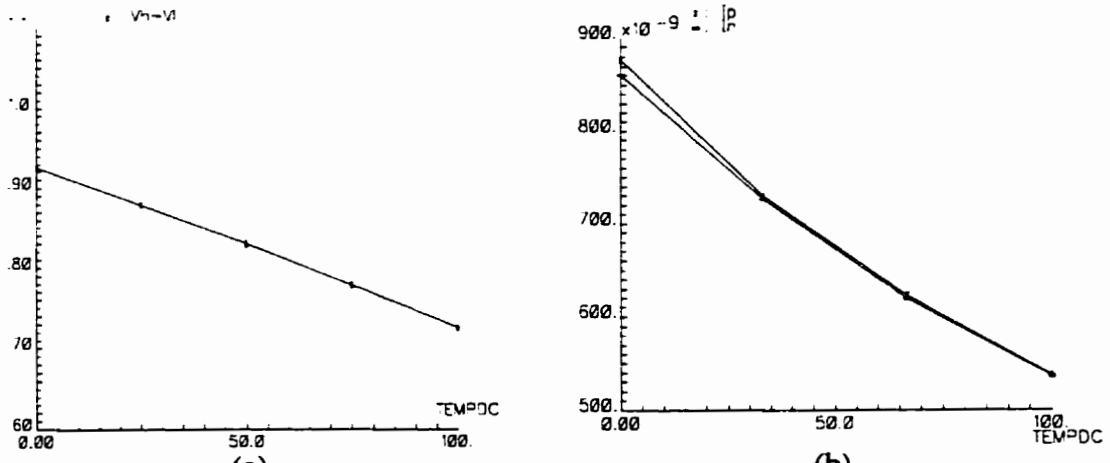


Fig. 13. Variation of the temperature sensor voltage reference (a) and current reference (b) versus chip temperature (TEMPDC).

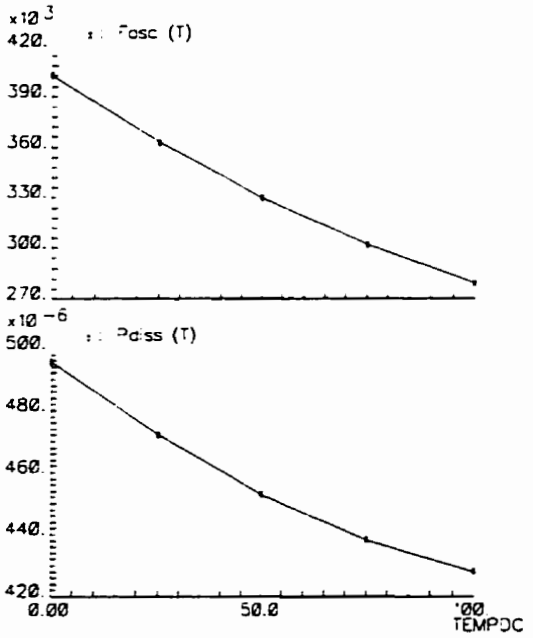


Fig. 14. Oscillation frequency and power dissipation of relaxation oscillator based temperature sensor.

The output voltage of the relaxation oscillator based temperature sensor and the effect of *En* signal is shown in Fig. 15.

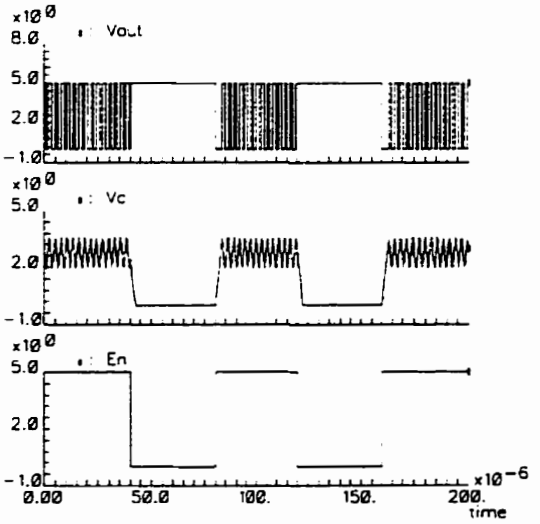


Fig. 15. Output signal of the relaxation oscillator-based temperature sensor.

5 Practical Issues and Discussion

In this paper, we have developed three slightly different chip temperature. The summary of important characteristics of these sensors is listed in Table 1. The second and third temperature sensors present better specification than the RC delay-controlled ring-oscillator-based temperature sensor except for the active chip area. As the sensitivity to V_{DD} of the second temperature sensor is low enough to be tolerated for the present application, one can prefer it over the third temperature sensor mainly because of its lower chip area and power dissipation. Its power dissipation can still be reduced by lowering the sensor nominal oscillation frequency. The right choice of the chip temperature sensors depends on the demand of application in terms of accuracy, silicon area, power dissipation, and sensitivity to V_{DD} variation.

Table 1: Summary of important characteristics of developed chip temperature sensors.

	DCRTS	**CCRTS**	**CCXTS**
Active Area	0.0174 mm^2	0.03 mm^2	0.0565 mm^2
Power Dissipation at 0 °C	0.86 mW	0.37 mW	0.49 mW
Sensitivity to V_{DD}	Medium	Low (– 0.22)	Not Sensitive (– 0.0)
Temperature Sensitive Element	Resistor	Resistor	Resistor
Suitable Technology	Any	Any	Any
Nominal Frequency at 0 °C	2.6 MHz	2.6 MHz	0.4 MHz

DCRTS: RC delay controlled ring oscillator temperature sensor, CCRTS: current-controlled ring oscillator-based temperature sensor, CCXTS: current-controlled relaxation oscillator-based temperature sensor.

A problem common to the proposed temperature sensors and eventually any temperature sensor is the uncertainty of the sensor output value due to the variation of the sensing element and other sensor elements which affect the sensor output with respect to the process variations. The problem stem from the fact that process and temperature variations affect the oscillation frequency in the same way and without after fabrication trimming it is impossible to differentiate the changes in sensor output due to the process and temperature variations. All high resolution temperature sensors presented in literature require after fabrication trimming [13]-[15]. The calibration procedure may be straight forward or very complicated depending to the temperature sensor architecture. In our case the sensing element is a resistor and therefore manual or laser resistor trimming, or on-chip digital calibration can be used.

The choice of trimming technique is up to the designer and the application demand. Laser trimming is especially attractive when the chip contains high quality analog circuits which must undergo a trimming procedure. In this case, the trimming of the temperature sensor resistor can be also performed at the same phase without a considerable additional cost. When a microcontroller or computational ability is already available on-chip, they can be reused for memory-based digital calibration of the sensor [14]. Otherwise, the manual resistor trimming can be performed to modify the resistor value by opening or closing some already considered and implemented switches by which a small resistor can be added to or removed from the original resistor.

A Monte Carlo analysis taking into account the tolerance value of the resistor and other circuit and technology parameters supplied by the manufacturer has been performed to estimate the uncertainty band of the oscillation frequency without any trimming for the first temperature sensor presented in this paper. To better visualize the results, the fast Fourier transform (FFT) of the output oscillating signal after the Monte Carlo analysis has

been presented in Fig. 16. A Gaussian distribution using 30 iterations has been used. The tolerance band of the oscillation frequency estimates the worst case deviation of the oscillation frequency from the expected nominal value after fabrication. The result predict that the worst case error of < -4 °C , +5 °C > can be expected without trimming. This error can be marginally acceptable for the application under investigation when no trimming procedure or calibration is available.

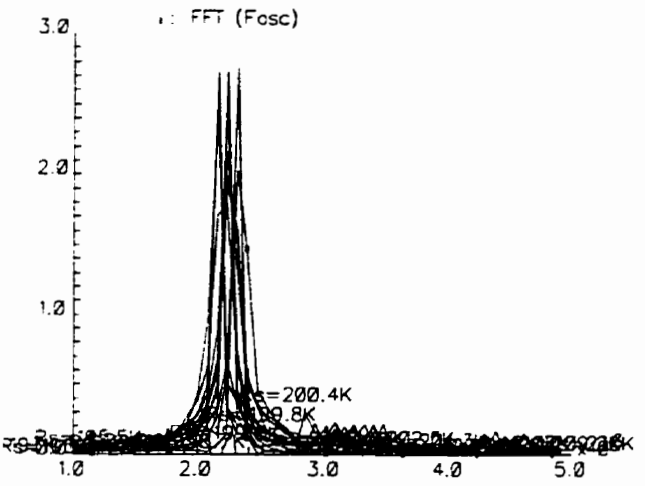


Fig. 16. Fast Fourier transform of the Monte Carlo analysis of the first temperature sensor (DCRTS) output signal.

Finally, it should be noted that in VLSI circuits many temperature sensors may be required to accurately map the thermal state of the microelectronic structure. The temperature sensors position is determined using tools that calculate the thermal state of the circuit under test based on current dissipated and circuit activity.

The last two temperature sensors proposed in this paper, can be divided into two sections: temperature-to-current converter and current-to-frequency converter either using

a current-controlled ring oscillator or a current-controlled relaxation oscillator. To minimize the area occupied by temperature sensors, the current-to-frequency converter can be common to all chip temperature sensors. In other words, all on-chip temperature-to-current converters interface to a single current-to-frequency converter. As the major area of the temperature sensor is occupied by its current-to-frequency converter, this technique will result in a considerable reduction in silicon area if many temperature sensors are required.

6 Experimental Results

Current-controlled temperature sensors have been fabricated using CMOS 1.2 μm technology of MITEL semiconductor. Fig. 17 illustrates the photomicrograph in which the upper circuit is the current-controlled ring oscillator-based temperature sensor and the lower circuit is the current-controlled relaxation oscillator-based temperature sensor.

To evaluate the deviation of the temperature sensors' nominal oscillation frequency at the room temperature 10 fabricated chips have been packaged and tested. The maximum deviation of the CCRTS's oscillation frequency at room temperature is 5% and that of the CCXTS's oscillation frequency is 4.5%. The oscillation frequency's nominal value for most of fabricated temperature sensors remain very close to the average of the nominal oscillation frequency. The variation of the oscillation frequency versus chip temperature corresponds to the simulation results and confirm a very good sensitivity of the oscillation frequency to the chip temperature. A sample output of both tempaerature sensors captured by a digital oscilloscope are presented in Fig. 18.

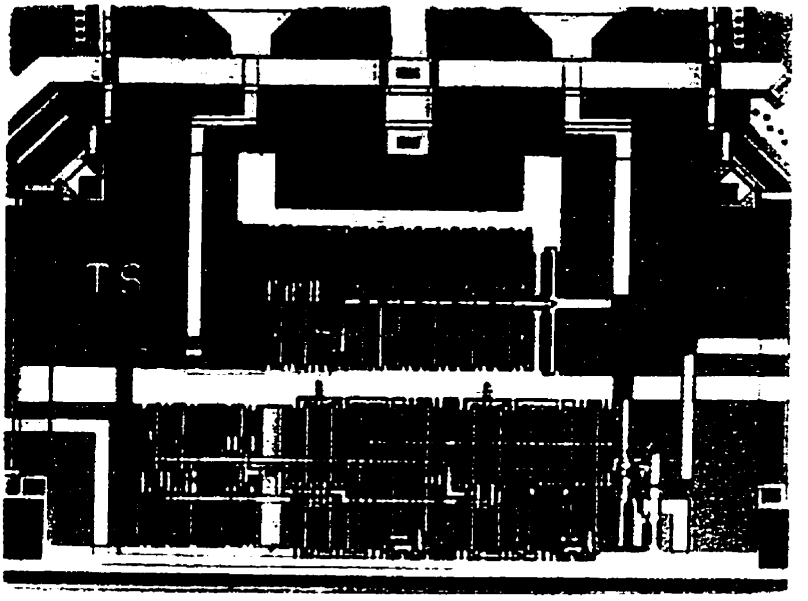
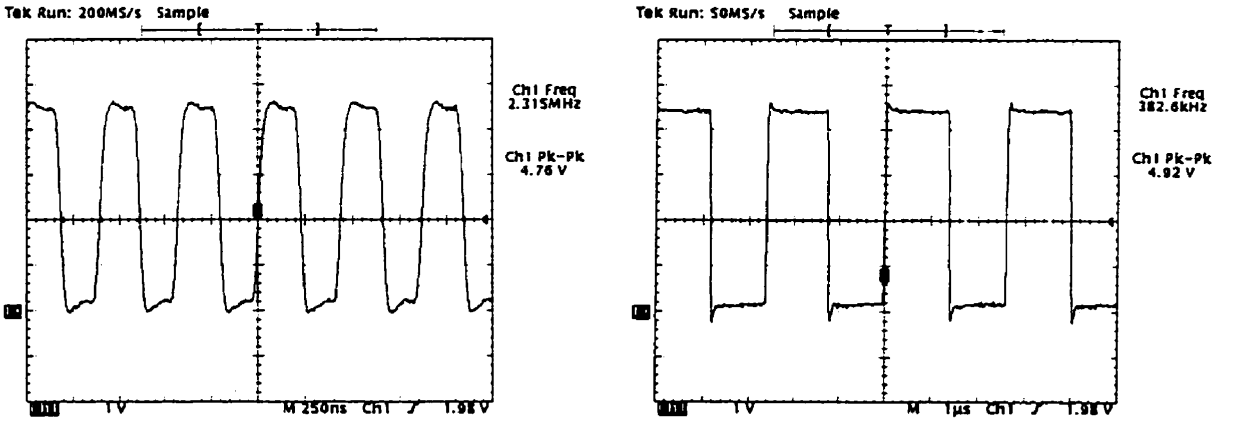


Fig. 17. Microscope photograph of the fabricated chip comtaining the CCRTS and CCXTS.



a) CCRTS b) CCXTS

Fig. 18. A typical output voltage of fabricated temperature sensors at room temperature.

7 Conclusions

In this paper, we have introduced practical and efficient built-in temperature sensors for thermal monitoring of integrated circuits. The main advantages of the presented chip temperature sensors are: low silicon area, low power dissipation, and digital output in form of oscillation frequency. Temperature sensors proposed in this paper can be implemented using regular digital process technologies and therefore can be easily implemented with any integrated circuits to increase their reliability. These sensors have been developed to support the oscillation-test strategy in order to increase the system reliability. We have just received a test chip containing current controlled ring and relaxation oscillator-based temperature sensors. Practical results from fabricated chips will be available soon and will be included in the final version of the paper. Other test sensors are under development to complete the family of sensors required for the oscillation-test method.

References

[1] Chandrakasan, A., S. Sheng, and R. Broderson, "Low-power CMOS Digital Design," *IEEE Journal of Solid-State Circuits*, 1992, pp. 473-484.

[2] Veendrick, H.J.M., "Short-Circuit Dissipation of Static CMOS Circuitry and its Impact on the Design of Buffer Circuits," *IEEE JSSC*, 1984, pp. 468-473.

[3] Arabi, K., and B. Kaminska, "Testing Analog and Mixed-Signal Integrated Circuits Using Oscillation-Test Method," To be appeared in *IEEE Transactions on Computer-Aided Design of Integrated Systems*.

[4] Arabi, K., and B. Kaminska, "Parametric and Catastrophic Fault Coverage of Analog Circuits Using Oscillation-Test Methodology," Proc. of the *IEEE VLSI Test Symp.*, Monterey, April 1997, pp. 166-171.

[5] Arabi, K., and B. Kaminska, "Oscillation-Test Strategy for Analog and Mixed-Signal Integrated Circuits," Proc. of the *IEEE VLSI Test Symp.*, 1996.

[6] Qunot, G.M., N. Paris, and B. Zavidovique, "A Temperature and Voltage Measurement Cell for VLSI circuits," Proc. of the *Euro-ASIC*, 1991.

[7] Bosch, B., "A Thermal Oscillator Using the Thermoelectronic (Seebeck) Effect in Silicon," *Solid-State Electronics*, vol. 12, 1976, pp. 372-373.

[8] Székely, V., and M. Rencz, "Thermal Test and Monitoring," Proc. of the *European Design and Test Conference*, 1995, p. 601.

[9] Meijer, G.C.M., "Thermal Sensors Based on Transistors," *Sensors and Actuators*, Vol. A10, 1986, pp. 103-125.

[10] Rasmussen, W., J.-Y Zhu, S. Richard, and D. Cheeke, "CMOS Intelligent Temperature Sensor," Proc. of the *IEEE 33rd Midwest Symp. Circuit and Systems*, 1990, pp. 849-852.

[11] Zhu, J.-Y, W. Rasmussen, S. Richard, and D. Cheeke, "Ultrastable Integrated CMOS Oscillator," *In'l. J. Electronics*, Vol. 70, 12991, pp. 433-441.

[12] Allen, P., and D.R. Holberg, "CMOS Analog Circuit Design," *Holt, Rineheart and Winston*, 1987.

[13] Meijer G.C.M., A.J.M. Boomkamp, and R.J. Duguesnoy, "An Accurate Biomedical Temperature Transducer with On-Chip Microcomputer Interfacing," *IEEE Journal* of *Solid-State Circuits*, vol. 23, No. 6, 1988, pp. 1405-1410.

[14] Bakker, A., and J.H. Huijsing, "Micropower CMOS Temperature Sensor with Digital Output," *IEEE Journal* of *Solid-State Circuits*, vol. 31, No. 7, 1996, pp. 933-937.

[15] Szajda, K.S., C.G. Sodini, and H.F. Bowman "A Low Noise, High Resolution Silicon Temperature Sensor," *IEEE Journal* of *Solid-State Circuits*, vol. 31, No. 9, 1996, pp. 1308-1313.

CHAPITRE 6

UN PROTOCOLE DE COMMUNICATION FIABLE POUR LA PROGRAMMATION ET TÉLÉMÉTRIE DES SYSTÈMES IMPLANTABLES

5.1 Résumé

La fiabilité de systèmes biomédicaux implantables est d'une importance majeure car ils sont destinés à des utilisations cliniques. L'un des problèmes principaux qui affaiblit la fiabilité du système est la communication avec l'implant. Si la perturbation affecte la communication, l'implant peut être mal programmé et par conséquent il ne fonctionnera pas comme on le désire. C'est pourquoi il est très important de prévoir un protocole de communication assurant la correction des erreurs jusqu'à une certaine probabilité assez basse d'avoir un message erroné. De plus, ce protocole de communication doit permettre de vérifier l'état de l'implant et celui du patient via un lien de télémétrie.

5.2 "A Reliable Communication Protocol for Externally Controlled Biomedical Implanted Devices"

Les techniques de codage de données se subdivisent en deux grandes catégories soient: la technique de détection d'erreurs et de répétition, sur demande, des messages erronés (ARQ: Antomatic Retansmission Request) et celle de la correction automatique des erreurs (FEC: Forward Error Correction). Puisque la technique ARQ exige un canal de

retour pour demander la retransmission, la technique FEC semble être un choix évident pour des systèmes qui ne se servent pas d'un canal de retour.

Dans la catégorie des codes-blocs, le code de Hamming a été préféré aux autres en raison de la simplicité des circuits nécessaires à la réalisation de son encodage et de son décodage. La stratégie de correction d'erreurs proposée dans ce chapitre permet de corriger plusieurs erreurs à la fois dans un message. L'article présentée dans ce chapitre est soumis pour publication dans *IEEE Transactions on Information Technology in Biomedicine*.

A Reliable Communication Protocol for Externally Controlled Biomedical Implanted Devices

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Abstract

We have developed a reliable communication protocol permitting an implant to recuperate safely the data and clock coming from external controllers over a noisy link. Two different FM demodulators and clock and data separators have been introduced to recover the incoming data and clock. The demodulators and data and clock separators can be fully implemented in regular CMOS technologies. A new forward error correction (FEC) strategy permitting multiple and burst error correction which is based on Hamming codes has been employed. Using a FEC technique, the correction procedure can be performed without retransmission. Hamming code is a linear block code and is an optimal choice because it has a satisfactory error correction performance with a very simple decoding hardware. The communication protocol presented in this paper can provide wireless communications for any implantable prosthesis. It has been designed and verified using CMOS 1.2μm technology of MITEL Semiconductor. The FEC architecture proposed for

multiple error correction has also been successfully implemented and tested in a XC7372 programmable device of Xilinx.

1 Introduction

Recent advances in miniaturization techniques made it possible to design advanced multifunction implantable prostheses which are used in clinical therapy for various type of disorders. Fig. 1 illustrates the general block diagram of biomedical implantable systems. This architecture can be customized to address the specific requirements of any application which requires an implant. The full system is based on inductive coupling technique for programming and powering the implant and optical coupling for telemetry. It includes an extracorporal controller and an implantable part. The external controller is used to control and reprogram the implant (read the state of patient, specify the stimulation algorithm, the waveform and pattern of stimulation and electrodes configuration, the quantity and cadence of drug to be delivered, etc.). It powers transdermally the implant via the inductive link during programming and stimulation. The implant is composed of a demodulator and voltage regulator to recuperate the incoming data and provide a stable power supply, a data and clock decoder module to recover synchronized data and clock, an internal controller which directs all operations of the implant, signal conditioning and telemetry modules to sample the biological information and send them to the physician and the internal controller to verify the state of the patient, and finally the output stage. A lithium battery is employed to power the embedded memory and the circuitry that must be always functional.

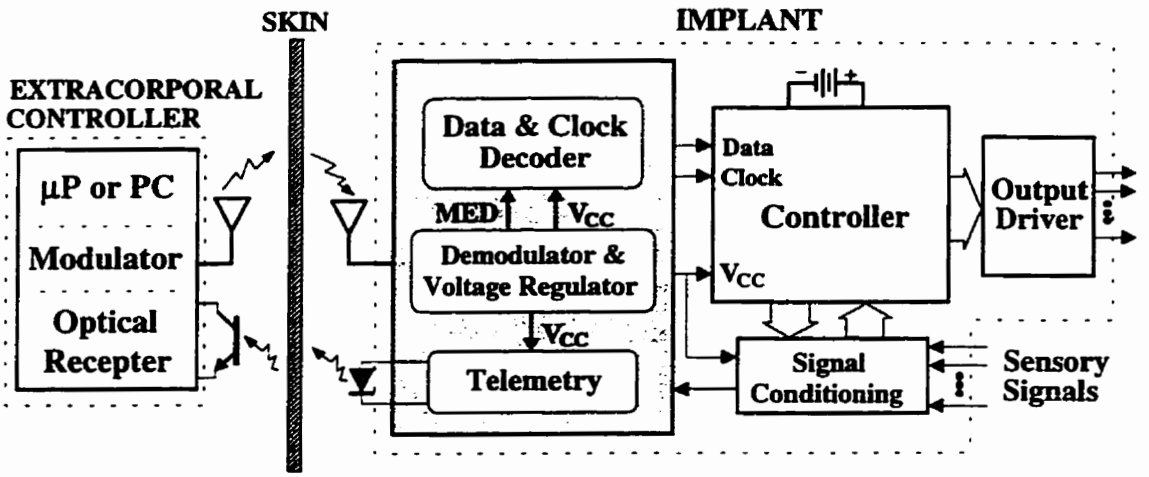


Fig. 1: General block diagram of a typical implantable system including its external controller.

Extracorporal controllers need to communicate with implanted systems for programming [2], delivering stimuli [4], and telemetery of clinical parameters [5] using wireless digital communications. As we are dealing with humans, the reliability of the communication is of great concern. The data transmitted to implant over a noisy link, programs the device and specifies the system configuration parameters and can affect the health of the implant host. Therefore, error detection and data verification become critical issues for the implantable systems. Unfortunately, the majority of existing implantable prostheses suffer from the lack of an error detection and correction protocol and are susceptible to noise [1].

This work aims at developing efficient demodulators, clock and data separators, and a secure communication protocol and the related architecture having multiple means of error detection and correction.

2 Demodulator and Data and Clock Decoder Design

In an implantable system, if the time base for the transmitter and the receiver are independent, a small differences between the two clocks become increasingly likely to cause errors due to sampling of the data at wrong time. To overcome this problem, data and clock are combined at the transmitter and are sent to the implant. A technique that has received considerable acceptance is called digital biphase or Manchester encoding. The biphase code provides strong timing information by providing a transition for every bit, whether it be a one or a zero. It also eliminates the residual DC problem, regardless of the message sequence, by providing both a positive and negative polarity for every bit. However, it requires twice the bandwidth of a bipolar signal and the error rate is doubled and it is difficult to decode. Manchester decoders utilize mixed digital-analog circuits and require a big capacitance that must be external.

Regarding the data communication technique, the majority of existing implants use the AM approaches [2]-[5] which are sensible to noise and other existing perturbations in communication channel. Furthermore, they are not appropriate for power transmission because of the amplitude variation that makes it more difficult for the voltage regulator block to provide a stable voltage source.

In this section, we investigate the use of FM technique for data and power transmission and polar return-to-zero (RZ) technique for data and clock encoding. FM is especially attractive because the carrier amplitude is not modulated by the incoming data and therefore the recovered supply voltage will be more stable. Fig. 2 illustrates the FM transmission of the binary message 10110100 encoded using polar RZ technique. Three different frequencies are used. As presented in Table 1, each frequency corresponds to a state of data and clock.

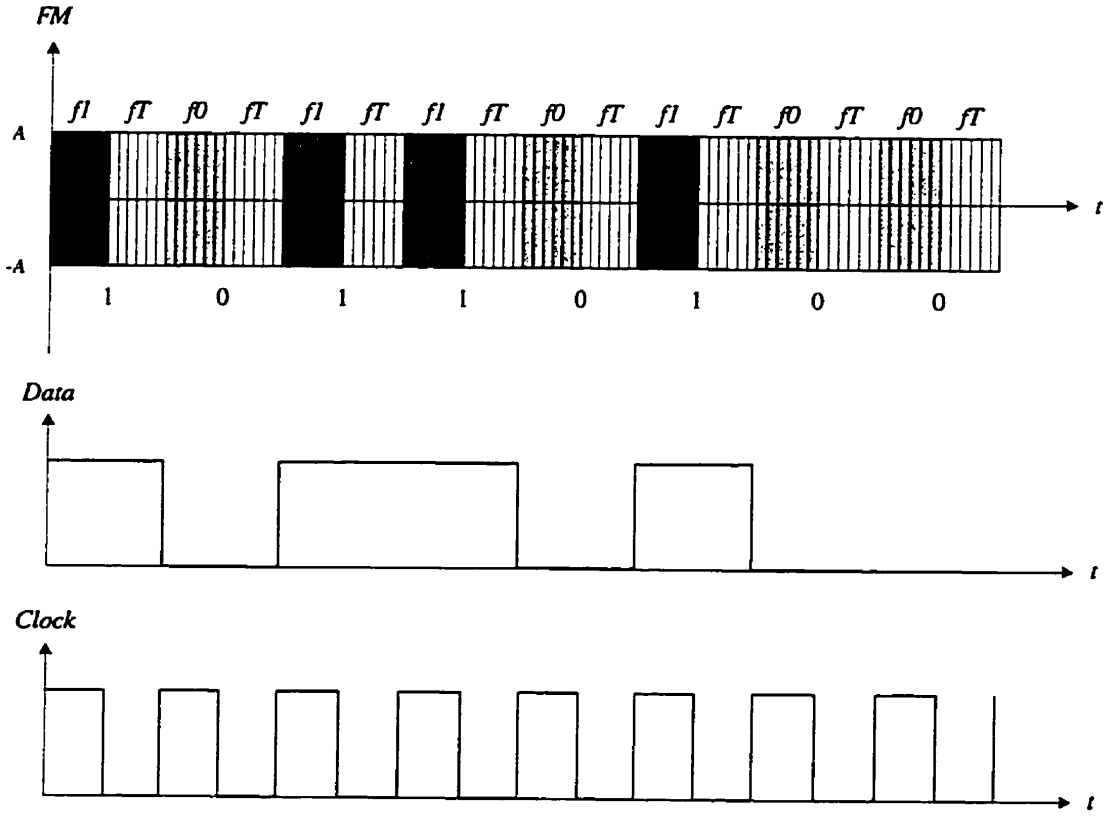


Fig. 2: Data encoding using polar RZ technique.

Table 1. Coding process of the FM transmission of polar RZ.

Frequency	**Data**	**Clock**
f1 (22 MHz)	1	1
f0 (18 MHz)	0	1
fT (20 MHz)	x	0

x could be logic 1 or 0.

In the following sections, two techniques for demodulation and data and clock separation are presented.

2.1 Phase-Locked Loop (PLL) demodulator

Digital or analog PLLs are usually used to regenerate the desired clock, and synchronize it to the rate of the received bit stream [8]-[11]. They are bulky or cause difficulties in monolithic implementation using standard digital CMOS process. We have designed a simple charge-pump PLL which is compatible with regular digital CMOS processes. The bloc diagram of a typical charge-pump PLL is depicted in Fig. 3. It includes a voltage controlled oscillator (VCO), a phase detector (PD), a charge-pump, and a loop filter.

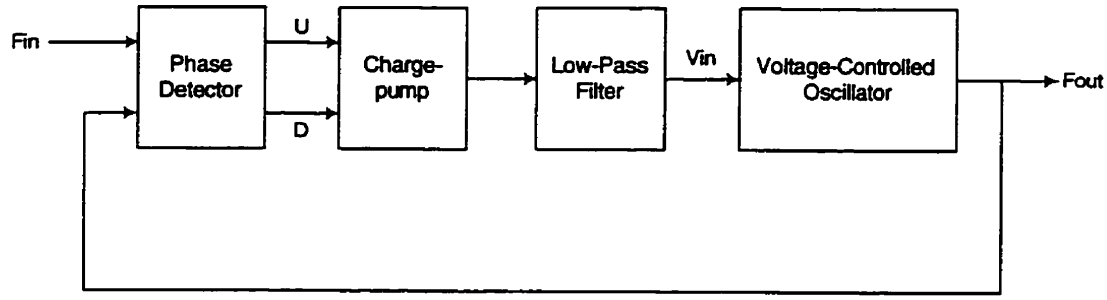


Fig. 3: Block diagram of a charge-pump digital PLL.

The phase detector is a conventional differential PD. The schematic of the charge-pump, the low-pass filter, and the VCO are represented in Fig. 4. The voltage-controlled oscillator is implemented as a simple current-controlled ring oscillator. The oscillation frequency is determined by the delay time of each inverter and the number of inverters in the loop. The delay time of each inverter is determined by the amount of current supply through the current source, the input capacitance, the threshold of the inverter.

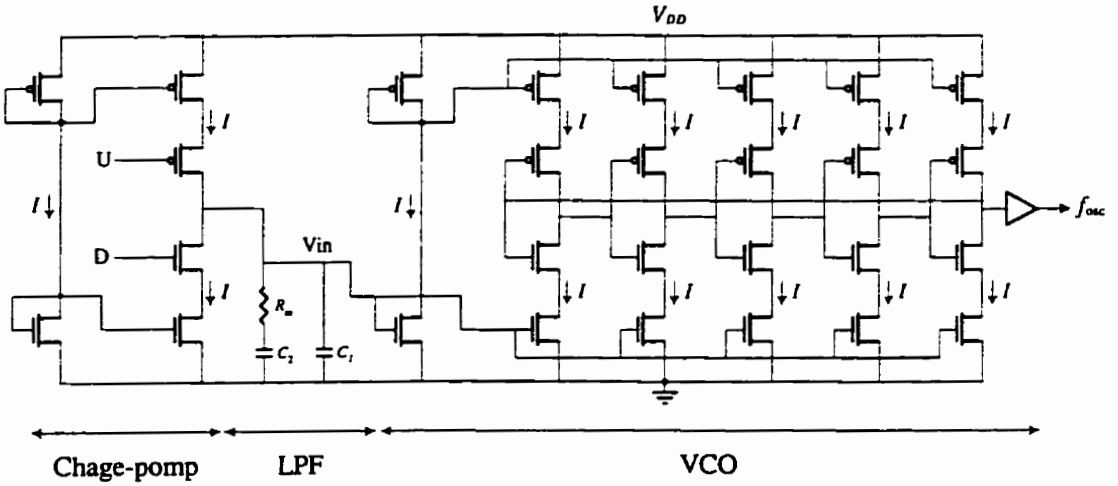


Fig. 4: Schematic diagram of some parts of the PLL.

The oscillator loop is composed of five inverters which establish a very high closed-loop gain to guarantee an instantaneous oscillation start-up. The output oscillation frequency of the VCO with respect to its input voltage is represented in Fig. 5.

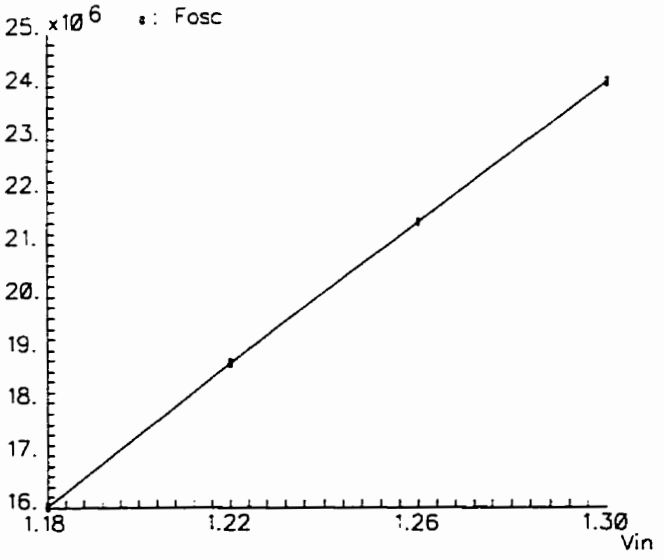


Fig. 5: VCO transfer function around 20 MHz.

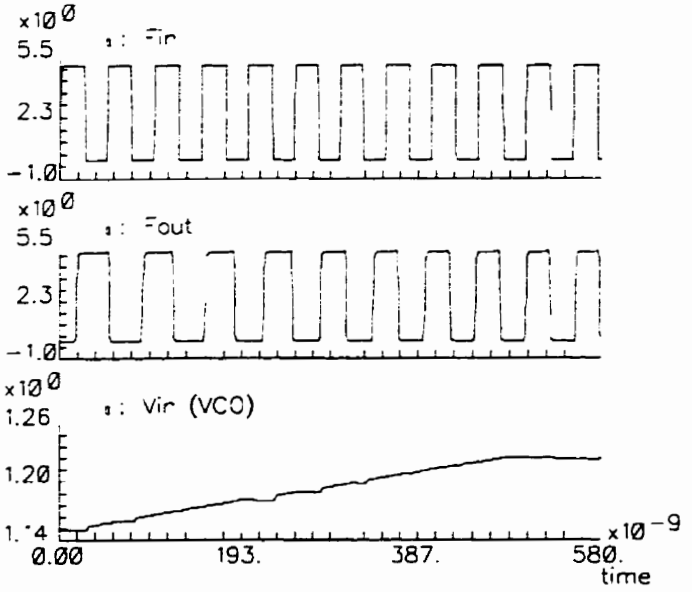


Fig. 6: PLL synchronization.

Fig. 5 depicts a simulation of the whole PLL when it is locking to an input frequency of 20 MHz. Based on the VCO's transfer function, each input frequency stabilizes the VCO input voltage at a specific value. By observing these voltages, the value of the input frequency can be detected. If V_{f1} denotes the VCO input voltage related to $f1$, V_{f0} denotes the VCO input voltage of $f0$ and V_{fT} denotes that of fT, the comparators reference input voltage can be calculated as follows.

$$V_{T1} = \frac{V_{f1} + V_{fT}}{2} \tag{1}$$

$$V_{T2} = \frac{V_{f2} + V_{fT}}{2} \tag{2}$$

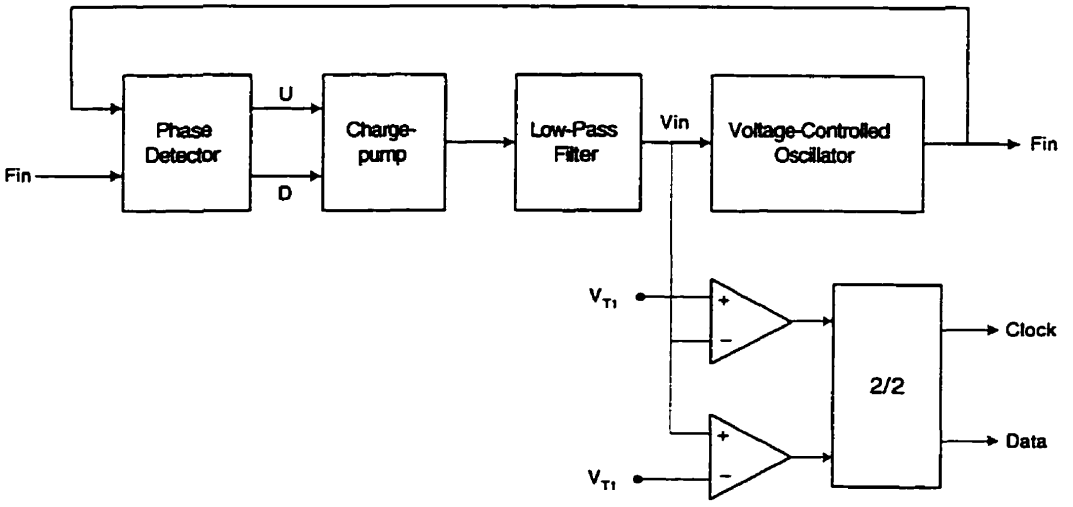


Fig. 7: Block diagram of the PLL-based demodulator.

2.2 Counter-Based Demodulator

The incoming FM signal can be demodulated using fully digital techniques such as using a counter to measure the value of the frequency. Fig. 8 shows the simplified circuit schematic of the proposed fully digital FM demodulator and data and clock separator. In this case, the input FM data is passed through a counter for a predetermined period of time.

The counter is enabled by the high level of a reference frequency (f_{REF}), and therefore during the high state of the reference frequency the counter counts. At the falling edge of f_{REF}, the value of counter is saved in the latch and after a small delay introduced by the buffer the counter is reset to zero. During the low state of f_{REF}, the counter is disabled and stops counting and the latch content which is a number related to its input frequency coming from the FM signal can be evaluated by the decoder. Therefore, an accurate frequency-to-number conversion is obtained. The accuracy of the system is determined by

the reference frequency f_{REF} and the bit number of the counter N. The digital output value of the latch after each conversion is given by

$$B_{1:N} = \frac{f_{IN}}{2f_{REF}} \tag{3}$$

This technique results in very good accuracy and satisfies the requirements of our application. The reference frequency f_{REF} is normally available in the in the implant for other purposes such as stimulus generation or control of timings.

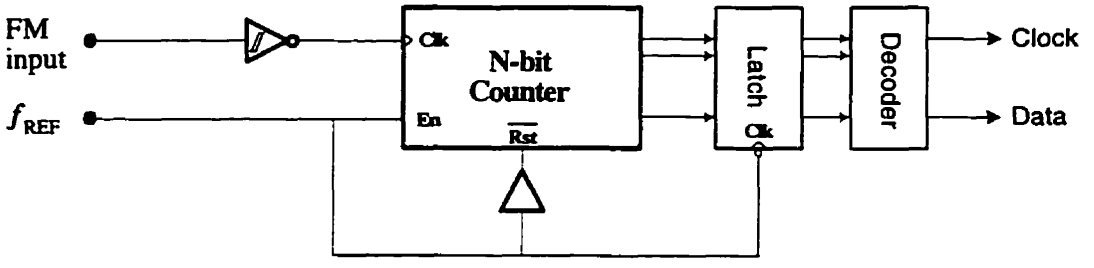


Fig. 8. Block diagram of the fully-digital FM demodulator and data and clock decoder.

Both of proposed FM demodulators and data and clock recovery techniques in this section are compatible with regular CMOS processes and occupy a relatively small silicon area in comparing with other realizations. An interesting advantage of the proposed techniques is that the demodulation and data and clock separation processes are effectuated at the same time.

3 Communication Protocol and Error Control Strategy

Implanted devices utilize either an inductive [2] or an optic link [4] In both cases, the data transferred to the implant are serially organized and transmitted using digital

communication techniques. Fig. 9 illustrates our proposed data frame from the external controller to the implant and vice versa. A header (key word) establishes the communication and data are sent serially followed by some stop bits to terminate the communication. The header is used to synchronize the data frame. Otherwise, the input noise could be mistaken for a message. Depending on the application, the communication between the implant and the external controller can be half or full duplex.

Fig. 9: Transmission/reception data frame for the communication protocol.

In order to reduce the transmission errors, and increase the reliability of the system, the data should be coded to provide FEC capability. FEC is based on creating redundancy in the data by adding some additional bits. In general, the higher the redundancy, the better the FEC capability. It should be noted that for the majority of applications a small volume of data is required to be communicated and therefore high degree of redundancy can be tolerated without affecting the communication efficiency.

Our error correcting strategy for each message word of 8-bits consist of two levels of FEC to provide the possibility of multiple error correction.

During the data encoding, first each message of 8-bits is partitioned in two 4-bit half messages and each of them is encoded using a conventional 7-bit Hamming code with a minimum distance of 3 (7,4) by adding three parity bits. Then, each bit is repeated three times to increase the data redundancy. Therefore, each message word of 8-bits is

transformed to a message of 42-bits. The procedure of encoding a message word of 8-bits is shown in Fig. 10 and equations (4).

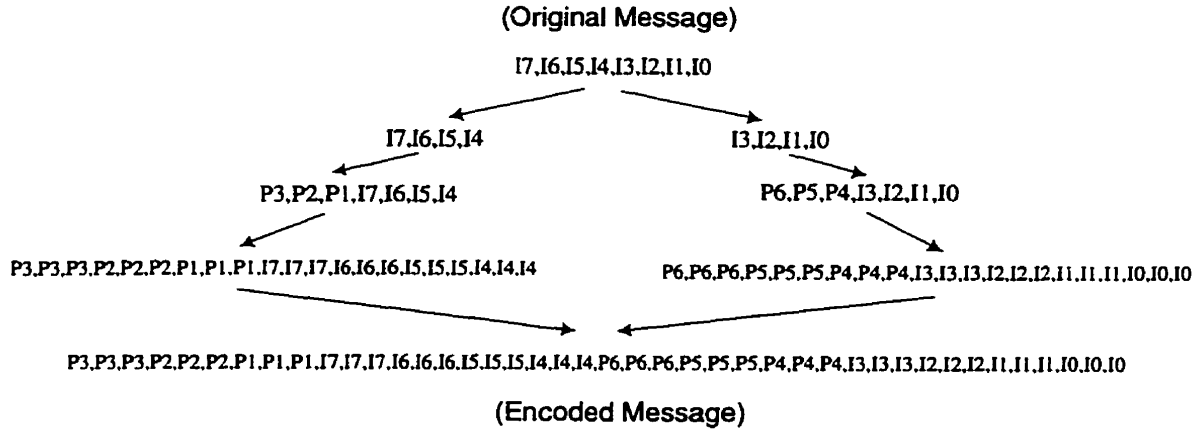


Fig. 10: Data flow of encoding procedure of an 8-bit message word.

At the transmitter, the check bits are determined from the following set of equations:

$$
\begin{aligned}
P1 &= I4 \oplus I5 \oplus I6 \\
P2 &= I5 \oplus I6 \oplus I7 \\
P3 &= I4 \oplus I5 \oplus I7 \\
\\
P4 &= I0 \oplus I1 \oplus I2 \\
P5 &= I1 \oplus I2 \oplus I3 \\
P6 &= I0 \oplus I1 \oplus I3
\end{aligned}
\qquad (4)
$$

As each bit is sent three times, a voter is used at the receiver to recover the bit using the majority rule. Therefore, at the first step, the voter circuitry performs the error correction and the result is sent for the second level of error correction. As a result, one bit error in each three bits can be corrected at this stage.

Each message word contains 4 information bits and 3 parity bits based on a conventional 7-bit Hamming code with a minimum distance of 3 (7,4). Therefore, at the second level of error correction one error over 7-bits can be corrected. This is equivalent to 2 to 3 bit error correction over a message of 21 bits.

Hamming code is a linear block code and is an optimal choice because it has a satisfactory error correction performance with a very simple decoding hardware. Other coding strategies such as cyclic and convolutional codes result in complicated decoding hardware [6],[7] which is not desirable in miniaturized implants. Using the proposed error correcting strategy, at least 18 bit errors per each message of 42 bits can be corrected and therefore the probability of an undetected error is the same as the original probability of error in 19 or more bits of a message of 42-bits. The probability of error in n or more bits of an N bit command word can be calculated using binomial distribution as follow:

$$p_n = \sum_{i=n}^{N} \frac{N!}{i!(N-i)!} (p_1)^i (1-p_1)^{(N-i)} \tag{5}$$

where p_1 is the probability of an error in any one bit and p_n is the probability of error in n-bits out of N-bits. In our case, up to 18 errors can be corrected and therefore the probability of an undetected error is reduced to the probability of having 19 errors in a message of 42-bits. Hence, neglecting the probability of errors in 20-bits and more, the new probability of error can approximately be calculated as follows:

$$p_{19} \approx 4.47\times10^{11}(p_1)^{19}(1-p_1)^{23} \approx 4.47\times10^{11}(p_1)^{19} \tag{6}$$

It should be noted that p_1 is normally very smaller than 10^{-5} which results in $p_{19} \approx 4.47\times10^{-84}$. Using the proposed error correction strategy, a burst error of up to 8-bits can

be corrected. Considering the worst case, up to three bits of error in each half portion of a message can be corrected.

4 Design of Error Correction Module

At the implant, upon the reception of a valid header (key word), the incoming bit stream is shifted into a serial to parallel converter; then on time FEC is performed.

Fig. 11 depicts the block diagram of the proposed error corrector module. In the first level of error correcting a voter circuitry is used and for the second level of decoding syndrome calculation technique [6] is used for Hamming code decoding.. Other techniques like trellis decoding [7] are not suitable for hardware implementation and normally require soft decisions.

The implemented structure operates as follows. The serial to parallel converter 1 transforms the incoming serial bit to a 6-bit words to check the header. Once the header is detected, the signal SDF becomes active and the divider modulo 3 produces the signal Clk1 from the original Clk to sample the output of the voter block after each three clock cycles. The counter modulo 7, produces the signal Clk 2 from the clock signal Clk1 which is active when the content of the serial to parallel converter 2 is completed. Once, the serial to parallel converter 2 is full, the syndrome calculator generates the corrector vector ($S2\text{-}0$) or ($S'2\text{-}0$) from the received message $d7\text{-}1$, based on equations (7), indicating whether the received message contains an error or not.

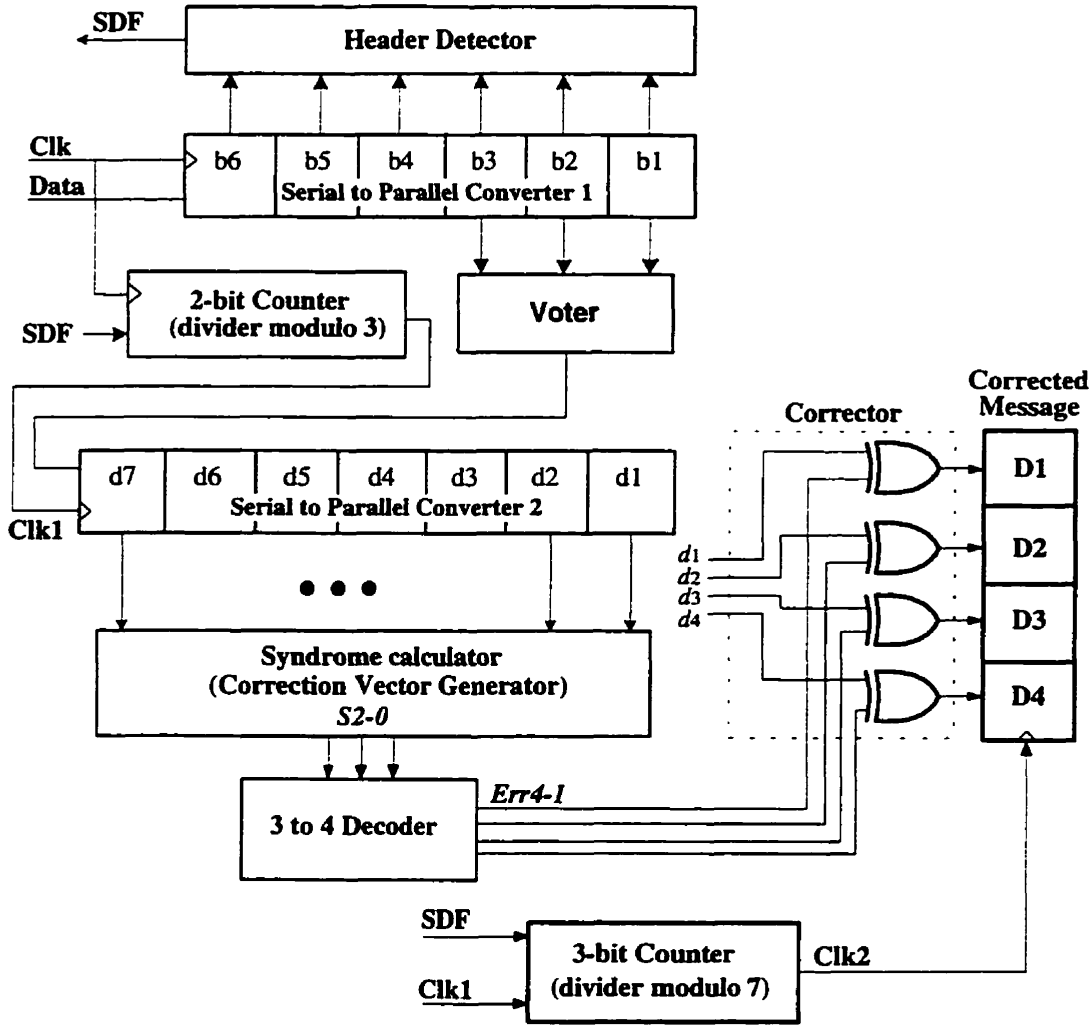


Fig. 11: Complete block diagram of the error corrector module. (SDF: Start of Data Frame).

The 3 to 4 decoder block looks up at the assumed error vector (*d4-1*) stored in the Table 2 which represents the relationship between the syndrome vector (*S2-0*) and the erroneous nit. Error vector addresses a single erroneous bit. The sum *d4-1* + *Err4-1* implemented by the corrector (exclusive-OR gates) finally generates the corrected data. When a message word is completed the correcting procedure is accomplished in less than

one clock cycle and at the next clock cycle the signal Clk2 is activated to latch the corrected message (*D4-1*) in the output register.

$$
\begin{aligned}
S0 &= P1 \oplus I4 \oplus I5 \oplus I6 \\
S1 &= P2 \oplus I5 \oplus I6 \oplus I7 \\
S2 &= P3 \oplus I4 \oplus I5 \oplus I7 \\
\\
S'0 &= P4 \oplus I0 \oplus I1 \oplus I2 \\
S'1 &= P5 \oplus I1 \oplus I2 \oplus I3 \\
S'2 &= P6 \oplus I0 \oplus I1 \oplus I3
\end{aligned}
\qquad (7)
$$

If there are no errors then *S2-0* = (000) and so the received message is not affected. In order to minimize the hardware, the elements of error vector related to parity check bits have been omitted because they are of no further interest.

Table 2: Correction table for the (7,4) Hamming code with a minimum distance of 3

S2-0	**Erroneous Bit**	***S'2-0***	**Erroneous Bit**
000	none	000	none
001	P1	001	P4
010	P2	010	P5
011	I6	011	I2
100	P3	100	P6
101	I4	101	I0
110	I7	110	I3
111	I5	111	I1

The basic principle of a voter circuitry is very simple. The first two bits are compared together if they are similar, one of the is selected and passed to the output. If they are not equal, the third bit is passed to the output. The realization of the voter block is shown in Fig. 12.

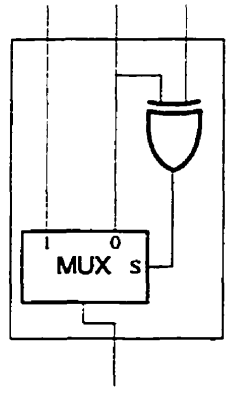


Fig. 12: Schematic of the voter block.

5 Results

The layout was generated using Cadence® tool based on CMOS 1.2 μm technology of MITEL Semiconductor. The proposed architectures occupy a very small area of silicon (*0.32 mm*^{2}) in comparing with other techniques [3],[6]-[11]. The errors injected during simulations were fully detected. The generated layout is illustrated in Fig. 13.

Small power dissipation is an important characteristic for implantable systems. The circuit has been especially optimized for low power. The architecture of the data and clock recovery is based on asynchronous design technique In an asynchronous digital circuit the number of transitions are minimized and the memory elements receive the clock just when they must perform a function. A prototype of the proposed error correction strategy has been implemented using a XC7372 EPLD of Xilinx which is a high performance reprogrammable complex PLD. 92% of available macrocells have been used. The practical results confirm the validity of the error correction technique proposed in this paper. Comparing the error correction strategy proposed in this paper with the previously reported technique in [3], the error correction capability is extremely higher and yet the area occupied by the proposed architecture is smaller.

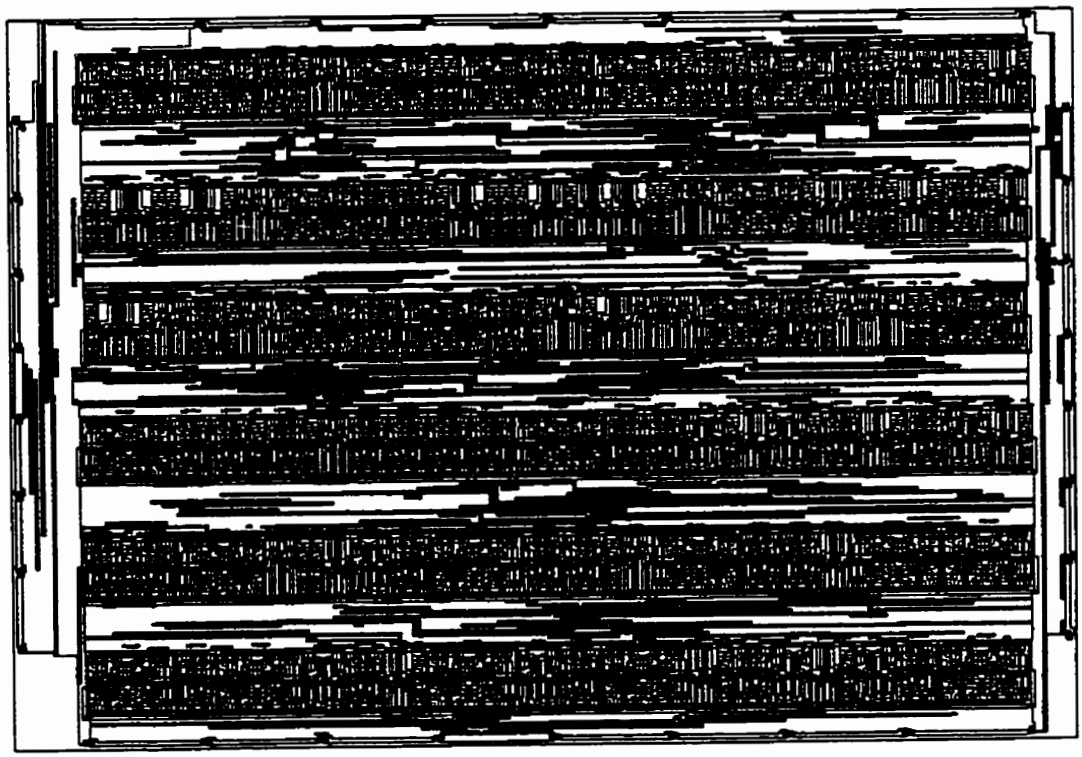


Fig. 13: Layout of the proposed error correction technique.

6 Conclusion

A new clock and data separator for programmable implanted devices has been proposed. The proposed fully digital data and clock separator requires a very small silicon area and can be easily integrated in regular CMOS processes. Besides, it does not need after fabrication trimmings. A forward error correction communication protocol for implantable prostheses using (7,4) Hamming code and triple bit transmission has been

presented. This module increases significantly the reliability of implants and protect them against existing noise in the data link. To our knowledge, it is the first error correcting architecture dedicated to implantable devices which is able to correct multiple errors in a message word. Its architecture is quite simple and requires a very small silicon area in comparing with other decoding techniques.

Acknowledgments

Authors would like to acknowledge the facilities provided by École de technologie supérieur to implement the communication protocol in a programmable device.

References

[1] Smith, S., and R. Aasen, "The effects of electromagnetic fields on cardiac pacemakers," *IEEE Trans. on Broadcasting.*, Vol. 38, No. 2, 1992, pp. 136-139.

[2] Arabi, K., and M. Sawan, "A multiprogrammable microstimulator dedicated to bladder dysfunctions," Proc. of the *IEEE EMBS*, Nov. 1994, Baltimore, pp. 974-975.

[3] Arabi, K., and M. Sawan, "A Secure Communication Protocol for Externally Controlled Implantable Devices," *Int. Conf. of the IEEE EMBS*, Sep. 1995.

[4] Smith, B., P.H. Peckham and W.K. Michael, "An externally powered, multichannel, implantable stimulator for versatile control of paralyzed muscle," *IEEE Trans. on Biomed. Eng.*, 1987, Vol. BME-34, No. 7, pp. 499-507.

[5] Miller, J.A., *et al.*, "Transcutaneous optical telemetry system for an implantable electrical ventricular heart assist device," *Journal of Med. & Biol. Eng. & Comput.*, 1992, Vol. 30, pp. 370-372.

[6] Lin, S., and D. Costello, "Error control coding: fundamentals and applications," *Prentice-Hall*, Englewood Cliffs, NJ, 1983.

[7] Honary, B., and G. Markarian, "Low complexity trellis decoding of Hamming codes," *Electronic Letters*, Vol. 29, No. 12, 1993, pp. 1114-1116.

[8] Bazes, M., and R. Ashuri, "A Novel CMOS Digital Clock and Data Decoder," *IEEE Jornal of Solid-State Circuits*, 1992., Vol. 27, No. 12, pp. 1934-1940.

[9] Kim, B., D. Helman, and P.R. Gray, "A 30-MHz Hybrid Analog/Digital Clock Recovery Circuit in 2-μm CMOS," *IEEE Jornal of Solid-State Circuits*, 1990, Vol. 25, No. 6, pp. 1385-1394.

[10] Guo, B., A. Hsu, Y.C. Wang, and J. Kubinec, "A 125 Mbs All-Digital Data Transceiver Using Synchronous Uniform Sampling," Proc. of the *IEEE ISSCC*, 1994, pp. 112-113.

[11] Saban, R., and A. Efendovich, "A Fully-Digital, 2 MB/sec, CMOS Data Separator," Proc. of the *IEEE ISCAS*, 1993, pp. 53-56.

CONCLUSION GÉNÉRALE

Dans cette thèse, nous avons exposé un problème pertinent qui est la fiabilité des systèmes biomédicaux implantables. Puisque les systèmes implantables fonctionnent à l'intérieur du corps humain, la fiabilité est un paramètre critique à observer. Toutes sortes de mauvais fonctionnement peuvent sérieusement affecter la vie ou le bien-être du patient. Un implant une fois implanté, est complètement inaccessible pour en apporter des ajustements ou modifications. De plus, le coût de procéder à des interventions chirurgicales pour détecter la source d'un mouvais fonctionnement de l'implant est assez élevé.

Nous avons développé des techniques de conception pour la testabilité et l'autovérification intégrée des circuits microélectroniques convenant aux systèmes implantables. Pour les circuits numériques, nous avons proposé un senseur de courant intégré afin de pouvoir appliquer le technique de test I_{DDQ}. Le senseur de courant présenté assure la précision de mesure et il n'affecte pas le niveau d'alimentation pour notre application. Le même senseur a été utilisé pour mesurer continuellement la consommation de puissance dans le circuit sous test. La mesure de consommation de puissance peut être considéré comme un test complémentaire au technique de test I_{DDQ}, car il vérifie la fonctionnalité du circuit sous le test durant le fonctionnement du circuit tandis que le technique de test I_{DDQ} test le circuit dans l'état de repos seulement. Le mesure de la consommation de puissance qui aide aussi à estimer la durée de vie des batteries utilisées pour alimenter le circuit dans des applications qui utilisent des batteries.

Pour les circuits analogiques et mixtes, on a développé des méthodes efficaces et simples pour l'autovérification intégré. Il a été démontré que ces techniques assurent une couverture de pannes assez élevée et requièrent une surface additionnelle très petite. Ces deux paramètres sont critiques pour les systèmes implantables car une fiabilité élevée et une surface de silicium petite sont des critères essentiels à respecter dans ce type des circuits. Nous avons adopté la technique de test par oscillation introduite tout récemment comme choix de méthode de test à cause de sa simplicité et l'efficacité qu'il nous offre pour l'implantation des structures pour l'autovérification intégrée.

Quant à l'interface bioélectronique des systèmes implantables, nous avons présenté des approches pratiques permettant de vérifier l'état de cette interface ainsi que l'état du tissu situé entre les électrodes. Il est nécessaire de remarquer que les problèmes mécaniques des interfaces bioélectroniques et le changement d'état du tissu situé entre les électrodes sont des causes importantes de mauvais fonctionnement de ces systèmes.

Dans le but d'augmenter la fiabilité des systèmes électroniques et surtout les circuits implantable, nous avons proposé d'utiliser des senseurs de températures intégrés pour vérifier l'état thermique de la puce dédiée. Les senseurs sont insérés dans les régions critiques de la puce. Une température élevée dans la région surveillée indique la possibilité éventuelle d'avoir des pannes dans le circuit intégré.

Un problème important qui est souvent négligé dans les systèmes implantables et celui de fiabilité de communication entre l'implant et le contrôleur externe. Nous avons proposé des architectures efficaces pour la démodulation et la récupération de l'horloge et les données dans un implant. De plus, afin d'augmenter la fiabilité de communication, une stratégie de correction d'erreurs a été proposée qui permet de corriger plusieurs erreurs à la fois dans un mot de message. La stratégie de correction d'erreur est unique dans le sens

qu'il corrige plusieurs erreurs à la fois en utilisant une architecture très simple et pratique pour les systèmes implantables.

Nous pouvons conclure que nous sommes parvenus à proposer des méthodes simples et efficaces qui permettent d'augmenter la fiabilité des systèmes implantables d'une façon substantielle. La plupart des techniques proposées ont été vérifiées en premier lieu par des simulations et par la suite en fabriquant des puces dédiées ou en réalisant des circuits avec des composants discrets. Les résultats expérimentaux et les simulations confirment l'efficacité des techniques proposées.

En adressant les problèmes de fiabilité des circuits implantables, cette thèse deviendra un pionnier et encouragera plusieurs recherches sur le problème soulevé. Une technique qui peut augmenter la fiabilité est de concevoir des circuits biomédicaux tolérants aux pannes. La conception des circuits biomédicaux tolérants aux pannes exige d'autres recherches détaillées. En effet, la conception des circuits numériques tolérants aux pannes est assez mature. Cependant, le problème n'a pas été encore abordé dans les circuits analogiques.

BIBLIOGRAPHIE

[1] A'AIN, A.K.B., BRATT, A.H. et DOREY, A.P. (1994). Testing Analog Circuits by Power Supply Voltage Control. Electronic Letters, 30, 214-215.

[2] AGNEW, W.F. et MCCREERY, D.B. (1990). Neural Prostheses: Fundamental Studies. Prentice Hall, Englewood Cliffs, N.J.

[3] AGRAWAL, V.D. (1992). Special Issue on I_{DDQ} Testing. Journal of Electronic Testing, Theory and Applications, 3.

[4] ALLEN, P. et HOLBERG, D.R. (1987). CMOS Analog Circuit Design. Holt, Rineheart and Winston.

[5] ARABI, K. et KAMINSKA, B. (1996). A New Technique to Monitor the Electrode and Lead Failures in Implantable Microstimulators and Sensors. Int'l. Conf. of the IEEE EMBS, Amsterdam.

[6] ARABI, K. et KAMINSKA, B. (1996). A Practical and Low-Cost Test Method to Design Reliable Implantable Systems. Int'l. Conf. of the IEEE EMBS, Amsterdam.

[7] ARABI, K. et KAMINSKA, B. (1996). Built-In Temperature and Current Sensors for On-line Oscillation Testing. 2nd IEEE Int. On-Line Testing Workshop, Saint-Jean de-Luz, 13-16.

[8] ARABI, K. et KAMINSKA, B. (1997). Design for Testability of Embeded Integrated Operational Amplifiers. Accepté pour la publication dans IEEE Journal of Solid-State Circuits.

[9] ARABI, K. et KAMINSKA, B. (1996). Design for Testability of Integrated Operational Amplifiers Using Oscillation-Test Strategy. IEEE Int'l Conf. on Computer Design, Austin, 40-45.

[10] ARABI, K. et KAMINSKA, B. (1997). Efficient and Accurate Testing of Analog-to-Digital Converters Using Oscillation-Test Method. IEEE ED&TC, Paris.

[11] ARABI, K. et KAMINSKA, B. (1997). Parametric and Catastrophic Fault Coverage of Analog Circuits Using Oscillation-Test Methodology. IEEE VLSI Test Symp. Monterey, 166-171.

[12] ARABI, K. et KAMINSKA, B. (1997). Built-In Current Sensor Design. Soumis au Journal of Analog Electronics and Signal Processing, Kluwer Academic Publishers.

[13] ARABI, K., et KAMINSKA, B. (1996). Built-In Temperature Sensors for On-line Thermal Monitoring of Microelectronic Structures. Accepté pour la publication dans Journal of Electronic Testing: Theory and Application (JETTA).

[14] ARABI, K. et KAMINSKA, B. (1996). Efficient and Accurate Built-In Self-Testing of Analog-to-Digital Converters Using Oscillation-Test Method. Soumis au IEEE Trans. on Instrumentation and Measurement.

[15] ARABI, K. et KAMINSKA, B. (1997). A BIST Scheme for Functional and Structural Testing of Analog and Mixed-Signal Integrated Circuits. IEEE Int'l Test Conference, Washington.

[16] ARABI, K. et KAMINSKA, B. (1996). Oscillation-Test Methodology for Low-Cost Testing of Active Analog Filters. Soumis au IEEE Trans. on Instrumentation and Measurement.

[17] ARABI, K. et KAMINSKA, B. (1996). Oscillation-Test Strategy for Analog and Mixed-Signal Integrated Circuits. IEEE VLSI Test Symp., Princeton, 476-482.

[18] ARABI, K. et SAWAN, M. (1995). Monolithic Miniaturized Programmable Implant for Neuromuscular Stimulation. Int'l. Conf. of the IEEE EMBS.

[19] ARABI, K. et SAWAN, M. (1995). A Novel CMOS Digital Clock and Data Decoder for Implantable Systems. Int'l. Conf. of the IEEE EMBS.

[20] ARABI, K. et SAWAN, M. (1995). A Secure Communication Protocol for Externally Controlled Implantable Devices. Int. Conf. of the IEEE EMBS.

[21] ARABI, K. et SAWAN, M. (1995). A Universal Flexible Functional Electrical Stimulation System. Int. Conf. on Electrostimulation, Vienna, 161-164.

[22] ARABI, K. et SAWAN, M. (1995). Multiprogrammable Stimuli Generator for Neuromuscular Electrical Stimulation. Int'l. Conf. of the IEEE EMBS.

[23] ARABI, K. (1994) Conception d'un microstimulateur neuromusculaire implantable destiné à la récupération de dysfonctions urinaires. *Mémoire de maîtrise*, École Polytechnique de Montréal, Canada.

[24] ARABI, K. et KAMINSKA, B. (1997). Testing Analog and Mixed-Signal Integrated Circuits Using Oscillation-Test Method. Accepté pour la publication dans IEEE Transactions on Computer-Aided Design of Integrated Systems.

[25] ARABI, K. et KAMINSKA, B. (1997). Design for Reliability of Biomedical Implantable Systems. IEEE Int'l Mixed-Signal Testing Workshop, Seatle.

[26] ARABI, K. et SAWAN, M. (1994). A multiprogrammable microstimulator dedicated to bladder dysfunctions. Int'l. Conf. of the IEEE EMBS, Baltimore, 974-975.

[27] ARABI, K. et SAWAN, M. (1995). Implantable Multiporogrammable Microstimulator Dedicated to Bladder Control. Journal of Med. & Biol. Eng. & Comput., 34, 9-12.

[28] ARABI, K., KAMINSKA, B. et RZESZUT, J. (1994). A Built-In Self-Test Approach for Medium to High Resolution D/A Converters. IEEE ATS, Nara, 373-378.

[29] ARABI, K., KAMINSKA, B. et RZESZUT, J. (1994). A New Built-In Self-Test Approach for Digital-to-Analog and Analog-to-Digital Converters. IEEE Int'l Conf. on Computer Aided Design, San Jose, 491-494.

[30] ARABI, K., KAMINSKA, B. et RZESZUT, J. (1994). BIST for Digital-to-Analog and Analog-to-Digital Converters. IEEE Design & Test of Computers, 13, 40-49.

[31] AVERY®, The Micturition Stimulator. Avery Laboratories Inc., Farmingdale, N.Y.

[32] BAK, M., GIRVIN, J.P., HAMBERCHT, F.T., KUFTA, C.V., LOEB, G.E. et SCHMIDT, E.M. (1990). Visual sensations produced by intracortical microstimulation of the human occipital cortex. Journal of Med. & Biol. Eng. & Comput., 28, 257-259.

[33] BAKKER, A. et HUIJSING, J.H. (1996). Micropower CMOS Temperature Sensor with Digital Output. IEEE Journal of Solid-State Circuits, 31, 933-937.

[34] BANERJEE, P., et ABRAHAM, J.A. (1982). Fault Characterization of VLSI MOS Circuits. IEEE Int'l. Conf. Circuits and Computers, 564-568.

[35] BARTLETT, J.R., DOTY, R.W., BARRY, B., LEE-NEGRAO, N. et OVERMAN, W.H. (1977). Deleterious effects of prolonged electrical excitation of striate cortex in macaques. Brain Behav. Evol., 14, 46-66.

[36] BAZES, M. et ASHURI, R. (1992). A Novel CMOS Digital Clock and Data Decoder. IEEE Jornal of Solid-State Circuits, 27, 1934-1940.

[37] BERGMANN, S. et ERIKSEN, B.C. (1986). Anal electrostimulation in urinary incontinence: technical description of a new device. Urol. Int., 41, 411-417.

[38] BERLEKAMP, E.R. (1980). The technology of error-correcting codes. Proc. IEEE, 68, 564-594.

[39] BERLEKAMP, E.R. (1983). The construction of fast, high-rate, soft decision block decoders. IEEE Trans. Inf. Theory, 29, 372-378.

[40] BERNSTEIN, A.D. et PARSONNET, V. (1983). Microcomputer and microprocessor applications in cardiac pacing. Medical Instrumentation, 17, 329-334.

[41] BEY, P.P. (1991). Autonulling MOS Bridge for Sensor Applications. Int'l Conf of the IEEE EMBS, 1595-1596.

[42] BLOEDEL, J.R., et EBNER, T.J. (1983). Cerebellar Stimulation for Spasticity. IEEE Eng. in Med. and Biol. Mag. 36-43.

[43] BOBBA, R. (1990). Fast Embedded A/D Converter Testing Using the Microcontrollers's Resources. IEEE ITC, 598-604.

[44] BOND, D. et YOUNG R. (1977). Electrophernic repiration in a patient with sleep induced apnea. J. Neurosurg. Nurs., 9, 118-121.

[45] BOSCH, B. (1976) A Thermal Oscillator Using the Thermoelectronic (Seebeck) Effect in Silicon. Solid-State Electronics, 12, 372-373.

[46] BRINDLEY, G.S. (1977). An Implant to Empty the Bladder or Close the Urethra. J. of Neurology, 40, 358-369.

[47] BROWING, C. (1985). Testing A/D converters on Microprocessors. IEEE ITC, 818-824.

[48] CHANDRAKASAN, A., SHENG, S. et BRODERSON, R. (1992). Low-power CMOS Digital Design IEEE Journal of Solid-State Circuits, 473-484.

[49] COBBOLD, R.S.C. (1985). Transducers for Biomedical Measurements: Principles and Applications. John Wiley & Sons, Inc., New-York, Chap. 9 &10.

[50] COOPER, J.P. et SALMONS, S. (1988). Simple three-program implantable muscle stimulator with optical control. J. Biomed. Eng., 10, 467-469.

[51] CORCORAN, J.J., HORNAK, T. et SKOV, P.B. (1975). A High-Resolution Error Plotter for Analog-to-Digital Converters. IEEE Trans. on Instrumentation & Measurement, 24, 370-374.

[52] CRAGO, P.E. (1983). Control of Movements by Functional Neuromuscular Stimulation. IEEE Eng. in Med. and Biol. Mag. 32-36.

[53] CRAGO, P.E., MORTIMER, T. et PECKHAM, H. (1980). Closed-Loop Control of Force During Electrical Stimulation of Muscle. IEEE Trans. Biomed. Eng., 27, 306-311.

[54] DEPLASSCHE, R.V., (1994). Integrated Analog-to-Digital and Digital-to-Analog Converters. Kluwer Academic Publishers, 240-262.

[55] DEVARAYANADURG, G. et SOMA, M. (1994). Analytical Fault Modeling and Static Test Generation for Analog ICs. IEEE ICCAD, 44-47.

[56] DOREY, A.P., et HIBBERT, J.B. (1991). Simplified Test Strategies for Analog ICs. European Test Conf., 494-495.

[57] DORMAN, M.G., PRISBE, M.A. et MEINDL, J.D. (1985). A Monolithic Signal Processor for a Neurophysiological Telemetery System. IEEE J. Solid-State Circuits, 20, 1185-1193.

[58] DYMOND, A.M. (1976). Characteristics of the Metal-Tissue Interface of Stimulation Electrodes. IEEE Trans. on Biomed. Eng., 23, 274-280.

[59] FASANG, P.P., MULINS, D. et WONG, T. (1988). Design for Testability for Mixed Analog/Digital ASICS. IEEE Custom Integrated Circuit Conf., 16.5.1-16.5.4.

[60] FERNALD, K.W., COOK, T.A., MILLER, T.K. et PAULOS, J.J. (1991). A Microprocessor-Based Implantable Telemetry System. IEEE Computer Mag., 23-30.

[61] FIDLER, J.K. (1984). Differential-Incremental-Sensitivity Relationships. Electronic Letters, 20, 626-627.

[62] GIELEN, G., WANG, Z. et SANSEN, W. (1994). Fault Detection and Input Stimulus Determination for the Testing of Analog Integrated Circuits Based on Power-Supply Current Monitoring. IEEE ICCAD, 495-498.

[63] GUO, B., HSU, A., WANG, Y.C. et KUBINEC, J. (1994). A 125 Mbs All-Digital Data Transceiver Using Synchronous Uniform Sampling. IEEE ISSCC, 112-113.

[64] GUYTON, A.C. (1991). Neuroscience: Anatomy & Physiology. .B. Saunders Company.

[65] HAMMING, R.W. (1950). Detecting and Error Correcting Codes. BST Journal, 29, 147-160.

[66] HERIQUES, B.G. et FRANCA, J.E. (1993). High-Speed D/A Conversion with Linear Phase Sinx/x Compensation. IEEE ISCAS, 2, 1204-1207.

[67] HOCHMAIR-DESOYER, I.J. et HOCHMAIR, E.S. (1980). An eight-channel scala tympani electrode for auditory prostheses. IEEE Trans. Biomed. Eng., 27, 44-50.

[68] HONARY, B. et MARKARIAN, G. (1993). Low complexity trellis decoding of Hamming codes. Electronic Letters, 29, 1114-1116.

[69] HWANG, C., ISMAIL, M. et DEGROAT, J.E. (1996). On-Chip I_{DDQ} Testability Schemes for Detecting Multiple Faults in CMOS ICs. IEEE Journal of Solid-State Circuits, 31, 732-739.

[70] JI, J. et WISE, K.D. (1992). An Implantable CMOS Circuit Interface for Multiplexed Microelectrode Recording Arrays. IEEE J. of Solid-State Circuits, 27, 433-443.

[71] JOLLY, R.D. et MCCHARLES, R.H. (1982). A Low-Noise Amplifier for Switched Capacitor Filters. IEEE Journal of Solid-State Circuits, 17, 6, 1192-1194.

[72] KELLY, D.D. (1985). Central representations of pain and analgesia. Princiles of Neural Science, Kandel, E.K. et Schwartz, J., Elsevier, 331-343.

[73] KERSTER, W.A. (1978). Characterizing and Testing A/D and D/A Converters for Color Video Applications. IEEE Trans. on Circuits & Systems, 25, 539-550.

[74] KIM, B., HELMAN, D. et GRAY, P.R. (1990). A 30-MHz Hybrid Analog/Digital Clock Recovery Circuit in 2-μm CMOS. IEEE Journal of Solid-State Circuits, 25, 1385-1394.

[75] LACAVA, W., PANTISKAS, C. et MORSE, W. (1994). Monitoring Pacemaker Patients. Journal of Clinical Eng., 19, 39-46.

[76] LAKSHMIKUMAR, K.R. et HADAWAY, R.A. (1985). A High Speed 8-Bit Current Steering CMOS DAC. IEEE CICC, 156-159.

[77] LIN, S. et COSTELLO, D. (1983). Error control coding: fundamentals and applications. Prentice-Hall, Englewood Cliffs, NJ.

[78] LOEB, G.E., ZAMIN, C.J., SCHULMAN, J.H. et TROYK, P.R. (1991). An Injectable Microstimulator for Functional Electrical Stimulation. Journal of Med. & Biol. Eng. & Comput., 29, NS13-NS19.

[79] LOEB, G.E. (1991). Injectable microstimulator for functional electrical stimulation. Int'l Conf. of the IEEE EMBS, 772-773.

[80] MALY, W. et PATYRA, M. (1992). Built-In Current Testing. IEEE Journal of Solid-State Circuits, 27, 425-429.

[81] MARLETT, M.J. et ABRAHAM, J.A. (1988). DC IATP-An-Iterative Analog Circuit Test Generation Program for Generating Single Pattern Tests. IEEE Int'l Test Conf., 839-844.

[82] MAX, S. (1989). Fast, Accurate and Complete ADC Testing. *IEEE ITC*, 598-640.

[83] MCNEAL, D.R. (1977). 2000 years of electrical stimulation. Functional Electrical Stimulation: Application in Neural Prostheses, Hamberecht, F.T. et Reswick, J.B., New York: Marcel Dekker, 3-35.

[84] MEIJER, G.C.M., BOOMKAMP, A.J.M. et DUGUESNOY, R.J. (1988). An Accurate Biomedical Temperature Transducer with On-Chip Microcomputer Interfacing. IEEE Journal of Solid-State Circuits, 23, 1405-1410.

[85] MEIJER, G.C.M., (1986). Thermal Sensors Based on Transistors. Sensors and Actuators, 10, 103-125.

[86] MELZACK, R. et WALL, P.D. (1965). Pain mechanisms: a flew theory. Science, 150, 971-979.

[87] MIKI, T. et NAKAMURA, Y. (1986). An 80-MHz 8-bit CMOS D/A Converter. IEEE Journal of Solid State Circuits, 21, 983-988.

[88] MILLER, J.A., BELANGER, G., SONG, I. et JOHNSON, F. (1992). Transcutaneous optical telemetry system for an implantable electrical ventricular heart assist device. Journal of Med. & Biol. Eng. & Comput., 30, 370-372.

[89] MILOR, L. et VINCENTELLI, A.S. (1990). Optimal Test Set Design for Analog Circuits. IEEE ICCAD, 294-297.

[90] MILOR, L. et VISVANATHAN, V. (1989). Detection of Catastrophic Faults in Analog Integrated Circuits. IEEE Trans. on Computer Aided Design, 8, 114-130.

[91] MIURA, Y. et KINOSHITA, K. (1992). Circuit Design for Built-In Current Testing. IEEE Int'l Test Conf., 873-881.

[92] MUGICA, J. (1990). Survol historique de la technologie de la stimulation cardiaque. RBM, 11, 221-224.

[93] NADEAU-DOSTIE, B. (1985). Design et évaluation d'un stimulateur nerveux multicanal destiné à une prothèse auditive. Thèse de Doctorat, Université de Sherbrooke, Canada

[94] NAYLOR, J.R. (1978). Testing Digital/Analog and Analog/Digital Converters. IEEE Trans. on Circuits and Systems, 25, 526-538.

[95] NICOLAIDIS, M., VARGAS, F. et COURTOIS, B. (1993). Design of BISCs for Concurrent Checking in Radiation Environments. IEEE Trans. on Nuclear Science, 1584-1590.

[96] NIGH, P. et MALY, W. (1990). Test Generation for Current Testing. IEEE Design & Test of Computers, 7, 26-38.

[97] NOBACK, C.R. et DEMAREST, R.J. (1981). The human Nervous System; Basic Principles of Neurobiology. McGraw-Hill.

[98] OFFECIERS, E., PEETERS, S., MOENECLAY, L., DURME, M.V., DIJKAMANS, P. et BOUCHATAOUI, I. (1993). An Implantable System for Functional Stimulation Used as a Cochlear Implant. Monitoring of Orthopedic Implants, Burny, F. et Puers, R., Elsevier Publishers B.V., 147-155.

[99] OHLETZ, M.J. (1991). Hybrid Built-In Self-Test (HBIST) Structure for Mixed Analog/Digital Integrated Circuits. 2nd European Test Conference, 307-316.

[100] PECKHAM, P.H., POON, C.W., KO, W.H., MARSOLAIS, E.B., et ROSEN, J.J. (1981). Multichannel Implantable Stimulator for Control of Paralyzed Muscle. IEEE Trans. Biomed. Eng., 28, 530-535.

[101] PERKINS, T.A. (1986). Versatile Three-Channel Stimulation Controller for Restoration of Bladder Function in Paraplegia. J. Biomed. Eng., 8, 268-271.

[102] QUNOT, G.M., PARIS, N. et ZAVIDOVIQUE, B. (1991). A Temperature and Voltage Measurement Cell for VLSI circuits. Euro-ASIC.

[103] RASMUSSEN, W., ZHU, J.-Y., RICHARD, S. et CHEEKE, D. (1990). CMOS Intelligent Temperature Sensor. IEEE 33rd Midwest Symp. Circuit and Systems, 849-852.

[104] RENOVELL, M., AZAIS, F. et BERTRAND, Y. (1995). A Design for Test Technique for Multi-Stage Analog Circuits. Asian Test Symposium, 113-119.

[105] ROCA, M. et RUBIO, A. (1992). Selftesting CMOS Operational Amplifier. Electronic Letters, 28, 1452-1454.

[106] RUBIO, A., FIGUERAS, J. et SEGURA, J. (1990). Quiescent Current Sensor Circuits in Digital VLSI CMOS Testing. Electronic Letters, 26.

[107] SABAN, R. et EFENDOVICH, A. (1993). A Fully-Digital, 2 MB/sec, CMOS Data Separator. IEEE ISCAS, 53-56.

[108] SANSEN, W. (1982). On the Integration of an Internal Human Conditioning System. IEEE J. of Solid-State Circuits, 17, 513-521.

[109] SANSEN, W., VEREECKEN, R., PUERS, B., FOLENS, G. et BAJN, N.T. (1987). A Closed Loop System to Control the Bladder Function. Int'l Conf. of the IEEE-EMBS, 1149-1150.

[110] SCHOUWENAARS, H.J. (1988). A Low Power Stereo 16-bit CMOS D/A Converter for Digital Audio. IEEE Journal of Solid-State Circuits, 23, 1290-1297.

[111] SCHOUWENAARS, H.J. (1986). A Monolithic dual 16-Bit D/A Converter. IEEE Journal of Solid-State Circuits, 21, 424-429.

[112] SEDAN, R. et LAZORTHES, Y. (1978). La neurostimulation électrique thérapeutique. Neurochirurgie, 24, 102-112.

[113] SELIGMAN, L.J. (1982). Physiological Stimulators: From Electric Fish to Programmable Implants. IEEE Trans. Biomed. Eng., 29, 270-284.

[114] SENANI, R. (1993). Simple Sinusoidal Oscillator Using Op-amp Compensation Poles. Electronic Letters, 29, 452-453.

[115] SHEALY, C.N. (1974). Transcutaneous stimulation for control of pain. Clin. Neurosur., 21, 269-277.

[116] SHEALY, C.N., MORTIMER, J.T. et RESWICK, J. (1967). Electrical inhibition of pain by stimulation of the dorsal column: preliminary clinical reports. Anesth. Analg., 46, 489-491.

[117] SHEN, T.L., DALY, J.C. ET LO, J.C. (1993). A 2-ns Detecting Time, 2-µm CMOS Built-In Current Sensing Circuit. IEEE Journal of Solid-State Circuits, 28, 72-77.

[118] SMITH, B., PECKHAM, P.H. et MICHAEL, W.K. (1987). An externally powered, multichannel, implantable stimulator for versatile control of paralyzed muscle. IEEE Trans. on Biomed. Eng., 34, 499-507.

[119] SMITH, S. et AASEN, R. (1992). The Effects of Electromagnetic Fields on Cardiac Pacemakers. IEEE Trans. on Broadcasting., 38, 136-139.

[120] SODEN, J., JERRY, M. et HAWKINS, C.F. (1996). I_{DDQ} Testing: Issues Present and Future. IEEE Design & Test of Computers, 61-65.

[121] SOMA, M. (1993). Fault Coverage of DC Parametric Tests for Embedded Analog Amplifiers. IEEE Int'l Test Conf., 566-573.

[122] SOMA, M., (1990). A Design-for-Test Methodology for Active Analog Filters. IEEE ITC., 183-192.

[123] SONG, M., LEE, Y. et KIM, W. (1993). A Clock Feedthrough Reduction Circuit for Switched-Current Systems. IEEE Journal of Solid-State Circuits, 28, 133-137.

[124] SOUDERS, T.M. et FLACH, D.R. (1979). An Automated Test Set for High-Resolution Analog-to-Digital and Digital-to-Analog Converters. IEEE Trans. on Instrumentation and Measurement, 28, 239-244.

[125] SOUDERS, T.M. et FLACH, D.R. (1981). An NBS Calibration Service for A/D and D/A Converters. IEEE ITC, 290-300.

[126] SOUDERS, T.M. et LECHNER, J.A. (1980). A Technique for Measuring the Equivalent RMS Input Noise of A/D Converters. IEEE Trans. on Instrumentation and Measurement, 29, 251-256.

[127] SOUDERS, T.M. et FLACH, D.R. (1979). An Automated Test Set for High Resolution Analog-to-Digital and Digital-to-Analog Converters. IEEE ITC, 390-400.

[128] STAPPER, C., ARMSTRONG, F. et SAJI, K. (1983). Integrated Circuit Yield Statistics. 71, 453-470.

[129] STEINHAGEN, W. et ENGL, W.L. (1978). Design of Integrated Analog CMOS Circuits –A Multichannel Telemetry transmitter. IEEE J. Solid-State Circuits, 13, 799-805.

[130] STEYAERT, M. et SANSEN, W. (1990). Low Power Monolithic Signal Conditioning System. IEEE J. of Solid-State Circuits, 25, 609-612.

[131] STOTTS, L.J., INFINGER, K.R., BABKA, J. et GENZER, D. (1989). An 8-bit Microcomputer with Analog Subsystems for Implantable Biomedical Application. IEEE J. Solid-State Circuits, 24, 292-299.

[132] SZAJDA, K.S., SODINI, C.G. et BOWMAN, H.F. (1996). A Low Noise, High Resolution Silicon Temperature Sensor. IEEE Journal of Solid-State Circuits, 31, 1308-1313.

[133] SZÉKELY, V. et RENCZ, M. (1995). Thermal Test and Monitoring. European Design and Test Conference, 600-601.

[134] TANG, J.-J., LEE, K.-J. et LIU, B.-D. (1995). A Practical Current Sensing Technique for I_{DDQ} Testing. IEEE Trans. on VLSI Sys., 3, 302-310.

[135] TARJAN, P.P., et BERSTEIN, A.D. (1984). An Engineering Overview of Cardiac Pacing. IEEE Eng. Med. & Biol. Mag., 10-14.

[136] TERAOCA, E. (1993). A Built-In Self-Test for ADC and DAC in a Single-Chip Speech CODEC. IEEE ITC, 791-796.

[137] TERRY, R., et DAVIES, L.G. (1974). Implantable cardiac pacer having adjustable operating parameters. U.S. Pattent 3 805 796.

[138] The Semiconductor Industry Association (1994). The National Technology Road Map for Semiconductors, San Jose.

[139] TONER, M.F. et ROBERTS, G.W. (1993). A BIST Scheme for an SNR Test of a Sigma-Delta ADC. IEEE Int. Test Conf., 805-814.

[140] VEENDRICK, H.J.M. (1984). Short-Circuit Dissipation of Static CMOS Circuitry and its Impact on the Design of Buffer Circuits. IEEE Journal of Solid-State Circuits, 468-473.

[141] WAGNER, K.D., et WILIAMS, T.W. (1988). Design for Testability of Mixed Signal Integrated Circuits. IEEE Int'l Test Conf., 823-829.

[142] WALLQUIST, K.M., (1995). On the Effect of I_{SSQ} Testing in Reducing Early Failure Rate. IEEE Int'l Test Conf., 910-914.

[143] WEY, C.-L. (1990). Built-In Self-Test Structure for Analog Circuit Fault Diagnosis. IEEE Transactions on Instrumentation and Measurement, 39, 517-521.

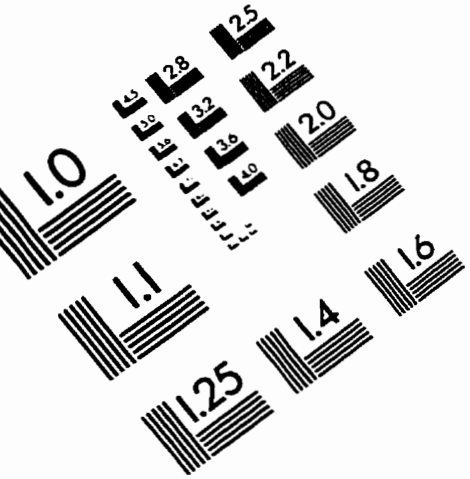
[144] WOUTER, D (1989). A Self-Calibration Technique for Monolithic High-Resolution D/A Converters. IEEE J. Solid-State Circuits, 4, 1517-1522.

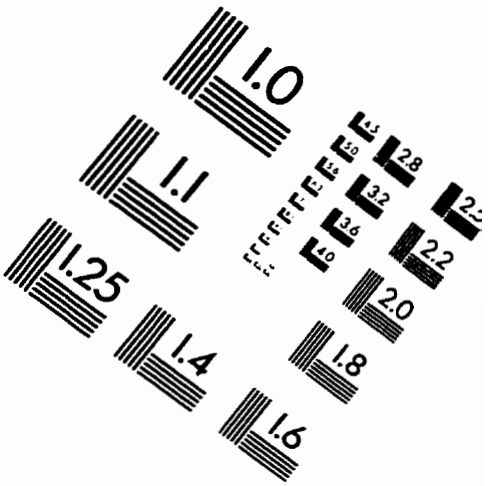
[145] YOO, H.-J. (1993). A Precision CMOS Voltage Reference with Enhancement Stability for the Application to Advanced VLSI's. IEEE ISCAS, 1318-1321.

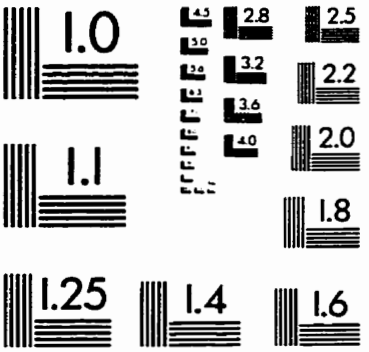
[146] ZHU, J.-Y., RASMUSSEN, W. RICHARD, S. et CHEEKE, D. (1993). Ultrastable Integrated CMOS Oscillator. In'l. J. Electronics, 70, 433-441.

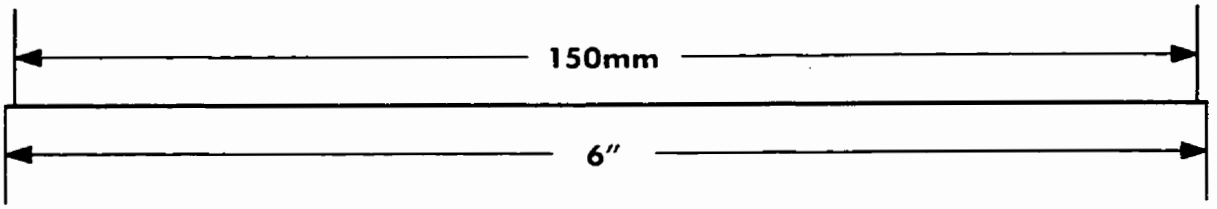
[147] ZIERHOFER, C.M., et HOCHMAIR, E.S. (1993). Cochlear implant for multichannel high-rate stimulation strategies. Int'l Conf. of the IEEE-EMBS, 1353-1354.

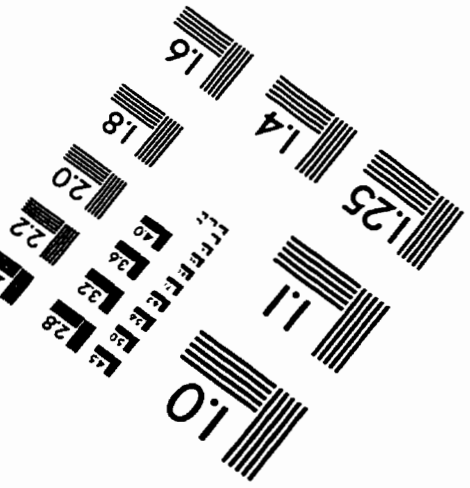
IMAGE EVALUATION
TEST TARGET (QA-3)

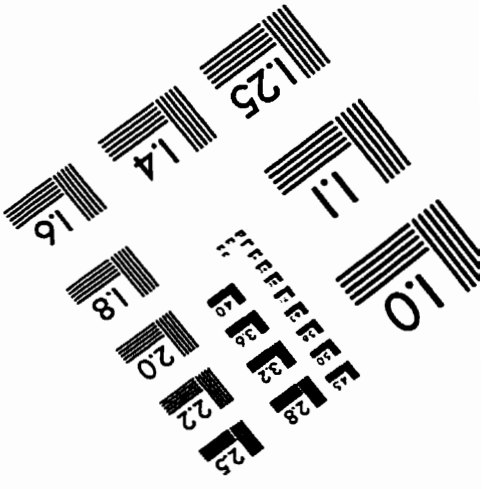












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